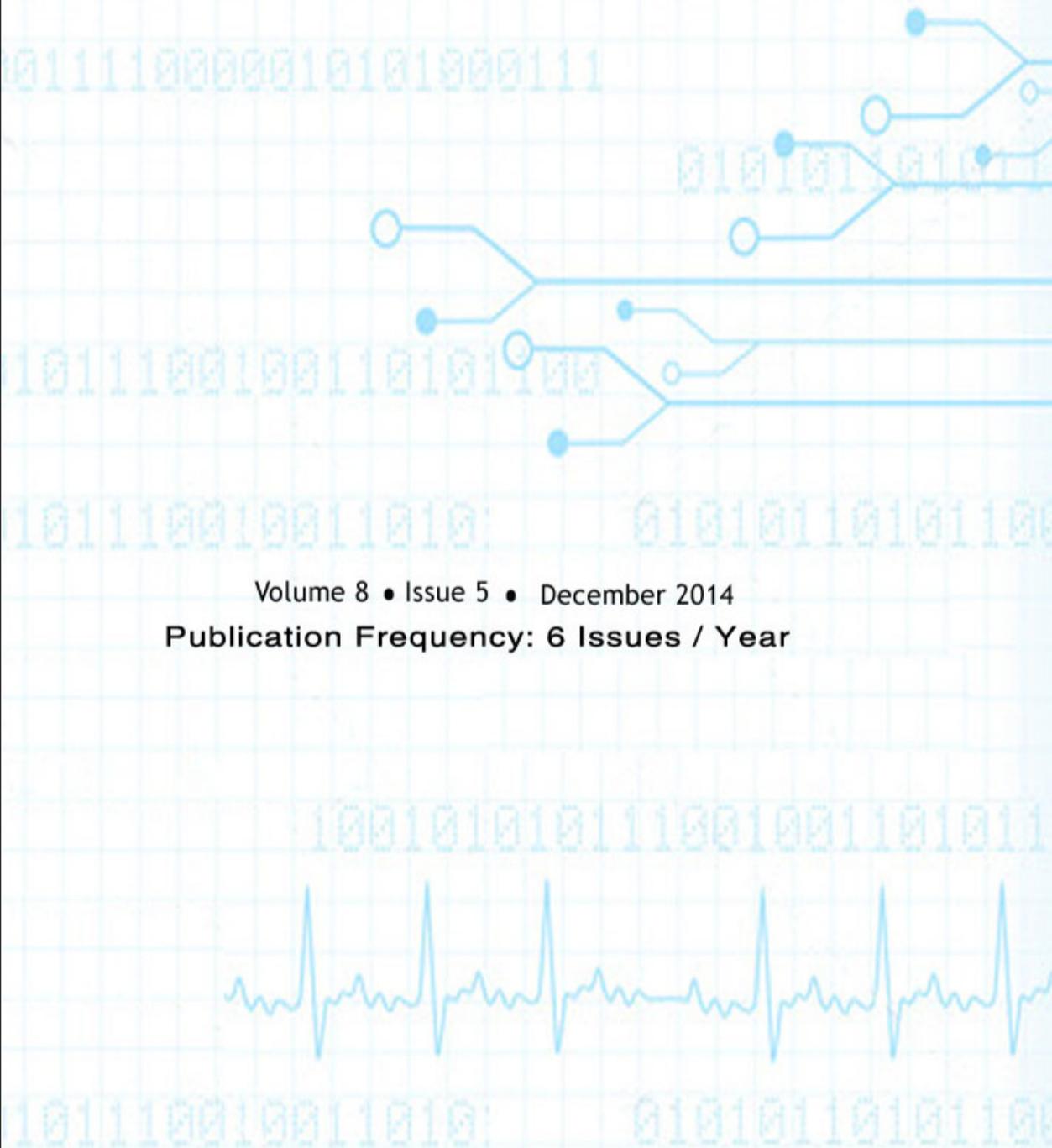


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# Image Resolution Enhancement Using Undecimated Double Density Wavelet Transform

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## Abstract

In this paper, an undecimated double density wavelet based image resolution enhancement technique is proposed. The critically sampled discrete wavelet transform (DWT) suffers from the drawbacks of being shift-variant and lacking the capacity to process directional information in images. The double density wavelet transform (DDWT) is an approximately shift-invariant transform capturing directional information. The undecimated double density wavelet transform (UDDWT) is an improvement of the DDWT, making it exactly shift-invariant. The method uses a forward and inverse UDDWT to construct a high resolution (HR) image from the given low resolution (LR) image. The results are compared with state-of-the-art resolution enhancement methods.

**Keywords:** Undecimated Double Density Wavelet Transform, Image Resolution, Stationary Wavelet, Resolution Enhancement.

---

## 1. INTRODUCTION

Image resolution enhancement is a usable pre-process for many satellite image processing applications, such as bridge recognition, building recognition and vehicle recognition. Image resolution enhancement techniques can be categorized into two major types according to the domain that they are applied in: 1) image domain and 2) transform domain. The techniques in the image domain use the statistical and geometric data directly extracted from the input image itself [1], [2], while transform-domain techniques use transformations such as decimated discrete wavelet transform (DWT) to achieve the image resolution enhancement [3]-[6]. The decimated DWT has been widely used for performing image resolution enhancement [3]-[5]. A common assumption of DWT-based image resolution enhancement is that the low-resolution (LR) image is the low pass filtered subband of the wavelet-transformed high-resolution (HR) image.

The image resolution is always a key feature for all kinds of images. With ever increasing size of the displays need for super resolution images has also been increased. This is also impacted by the limited size of the digital image sensor. Though widespread commercial cameras provide very high resolution images, generally the scientific cameras still have the resolution of only 512 x 512. Resolution enhancement has always been associated with the interpolation techniques.

Research suggests that interpolation methods increase the intensity of low frequency components. This means the interpolated image will have less number of sharp intensity transactions per pixel. A new method for resolution enhancement, which preserves high frequency contents of the image is suggested in the paper. Spatial domain techniques lag in the extraction and preservation of high frequency components of an image. This suggests that some other technique not involving spatial domain is to be used. So the image needs to be transformed to some other domain, processed and then converted back to the spatial domain. The domain can be Fourier domain, wavelet domain or any other. Fourier domain is more suitable for spectral filtering. The spectral filtering removes particular frequencies from the image. Wavelet domain separates components of an image into individual matrices. These matrices can be processed separately and combined together to get the desired result.

Fast algorithms for implementation of discrete wavelet transform have enhanced the use of the wavelet domain for image resolution improvement. Different image processing algorithms can be implemented with discrete wavelet transform (DWT). Double density wavelet transform (DDWT) decomposes an image into nine sub bands. These sub bands are of half the dimensions of that of image under consideration. Undecimated double density wavelet transform (UDDWT) is also being used for the image resolution enhancement. UDDWT has nine sub bands similar to DDWT but sub bands in UDDWT are of same size of that of the image. This paper proposes a new method for image resolution enhancement based on UDDWT.

In this paper, we compared the proposed method with various conventional methods for image resolution enhancement such as NEDI [1], HMM [7], DWT SR [8], DWT&SWT SR [9], LWT&SWT [10]. This comparison of various measures on images shows the dominance of the proposed method over existing methods.

## 2. DEVELOPMENT OF UNDECIMATED DOUBLE DENSITY WAVELET TRANSFORM

Although the DWT [11, 12, 13] is a powerful signal processing tool, it has two severe disadvantages:

1. Lack of shift-invariance, which means that minor shifts in the input signal, can cause major variations in the distribution of energy between wavelet coefficients at different scales
2. Since the wavelet filters are separable and real, it causes poor directional selectivity for diagonal features

The DWT is shift-variant because, the transform coefficients behave un-predictably under shifts of input signal, a problem that has been treated by introducing large amounts of redundancy into the transform to make it shift-invariant. The DWT has poor directional selectivity because it can only differentiate three different spatial-feature orientations. The DDWT is almost shift-invariant, multi-scale transform and has eight different spatial-feature orientations. Because the DDWT, at each scale, has twice as many wavelets as the DWT, it achieves lower shift sensitivity than the DWT. The undecimated Double Density Wavelet Transform follows the same filter bank structures of DDWT except the up sampling/down sampling process. Here at any given level in the iterated filter bank, this separable extension produces nine sub-bands in the same size as the original image. To indicate the filters used along the row and column dimensions to create the nine sub bands, the label of each of the sub-band is termed as  $h_x^i, h_y^j, i, j \in \{0,1,2\}$ . The subscript  $x$  indicates filtering along the rows, while subscript  $y$  denotes filtering along the columns. The superscripts 0, 1, 2 indicate the particular filter  $h_0(n), h_1(n), h_2(n)$  used to filter along a specified dimension to create the sub bands. Thus, at the end of the analysis filter bank, nine sub-bands will be obtained as shown in Fig. 1. In the UDDWT synthesis filter bank, the decomposed images are filtered using the filter coefficients  $g_0(n), g_1(n), g_2(n)$ . Fig. 2 illustrates

the synthesis filter bank structure, which composes the nine sub bands into a single image. In this work, the image decomposition and reconstruction is done by using the filters designed by Selesnick [14].

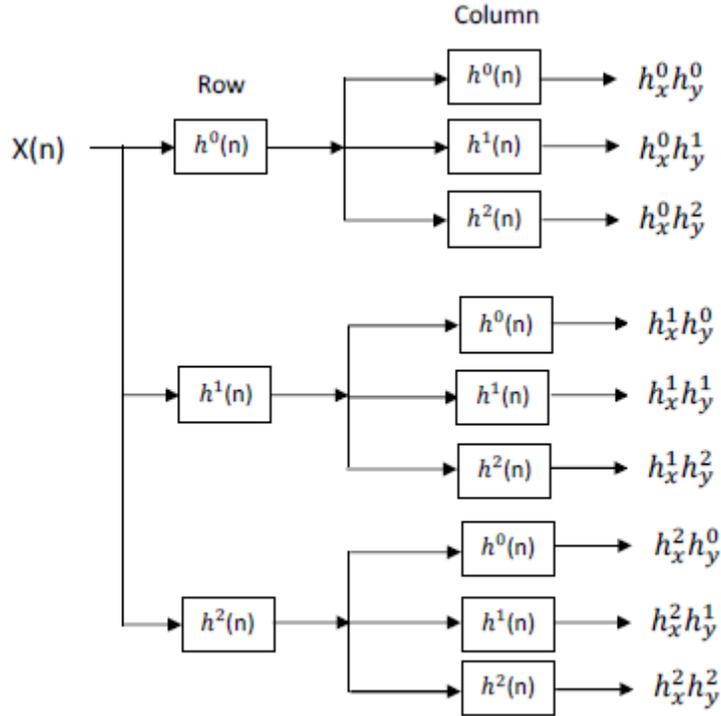


FIGURE 1: UDDWT analysis filter bank structure.

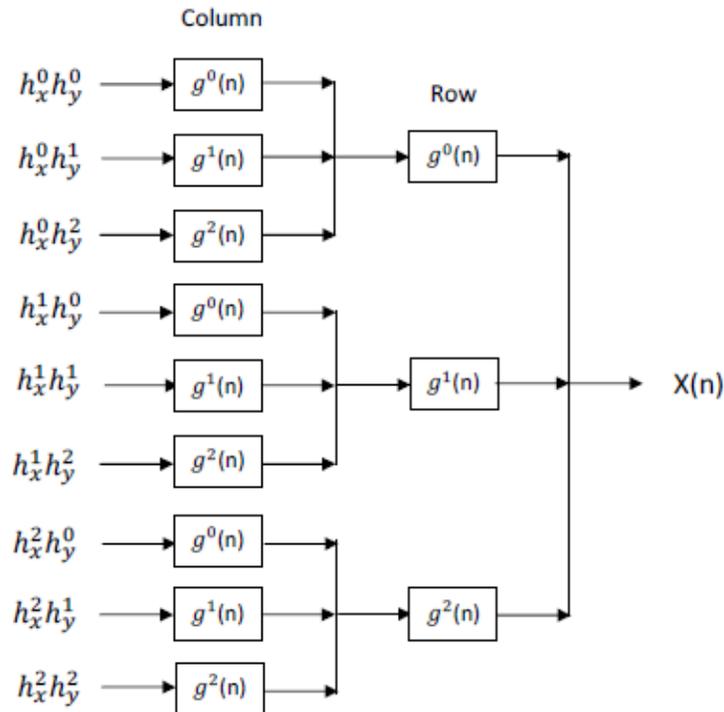


FIGURE 2: UDDWT synthesis filter bank structure.

### 3. PROPOSED METHOD

In the proposed method low resolution (LR) image is converted into a high resolution (HR) image by using UDDWT. First, apply DDWT and undecimated double density wavelet transform (UDDWT) on the input LR image. The DDWT produces 8 sub-bands which are decimated by factor 2 and an LPF component. Then all 8 subbands are interpolated by factor of  $\beta$ . Similarly UDDWT produces 8 sub-bands and an LPF component. Add corresponding subbands from each of DDWT and UDDWT as shown in Fig. 3. It is known that in the wavelet domain, lowpass filtering of the high resolution image produce the low resolution image. In other words, low frequency subband is the low resolution of the original image. Therefore, instead of using low frequency subband, which contains less information, the original image is used as the input to the inverse UDDWT. The quality of the super resolved image increases when using the input image instead of low frequency subband. Thus the output will be of higher resolution.

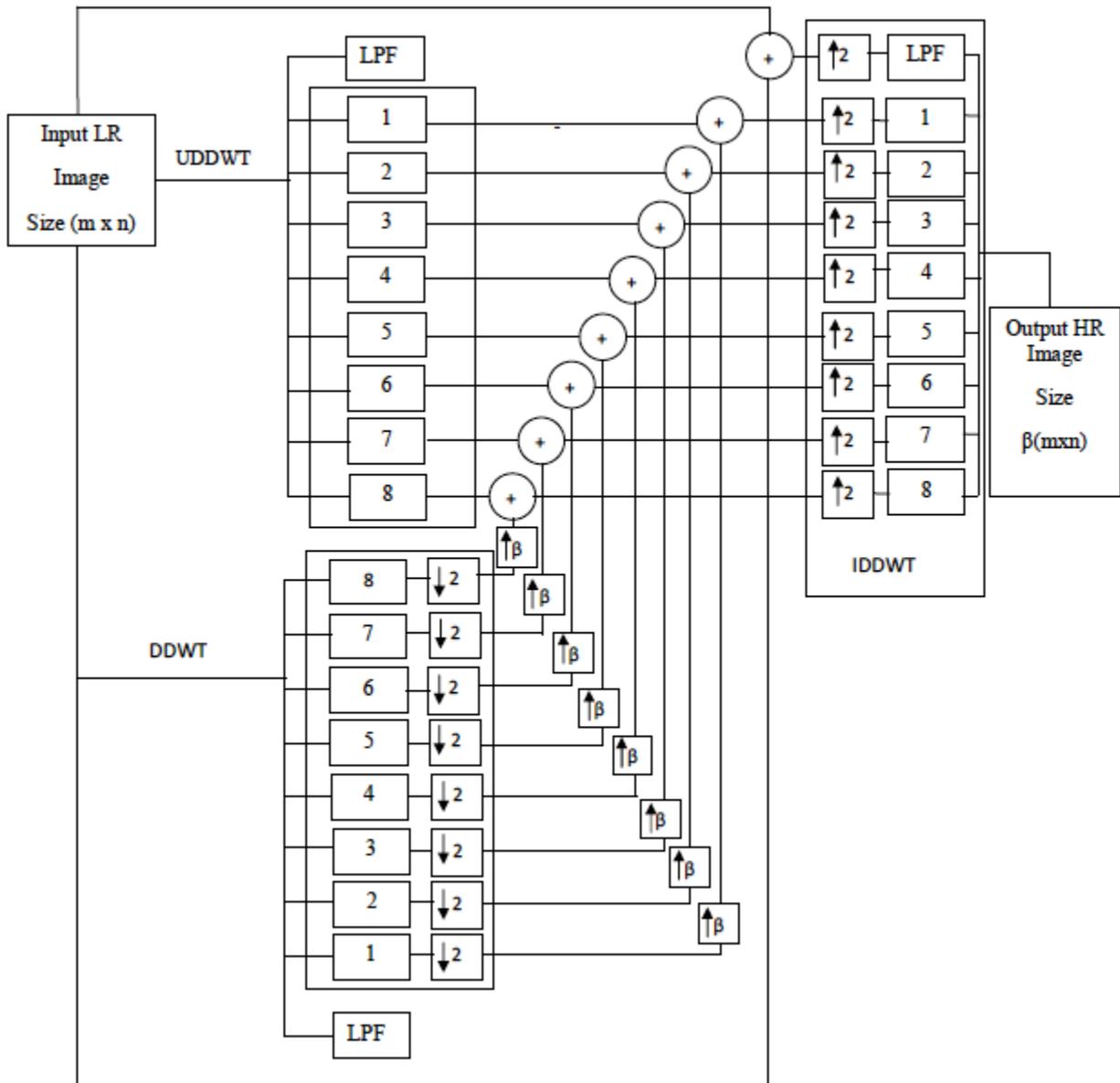


FIGURE 3: Proposed Method.

## 4. IMAGE QUALITY ANALYSIS

In this proposed work, the performance of the enhanced image is quantitatively analyzed by means of three measures such as peak signal to noise ratio (PSNR), Blind Image Quality Index (BIQI), and Visual Image Fidelity (VIF).

### 4.1. Peak Signal to Noise ratio (PSNR)

PSNR of the images is computed as

$$\text{PSNR} = 10 \log_{10} \left( \frac{I(m,n)_{\text{peak}}^2}{\text{MSE}} \right)$$

Where  $I(m,n)_{\text{peak}}$  is the peak pixel value in the image  $I(m,n)$  and usually is 255.

### 4.2. Blind Image Quality Index (BIQI)

BIQI [15] is also referred to as no reference image quality index. It refers to evaluating the quality of an image without the need of reference image or any training images. Images with no blur and noise offers higher BIQI value. Different parameters can be used to evaluate the quality of an image blindly.

### 4.3. Visual Image Fidelity (VIF)

VIF index [16] is the ratio of distorted image information to reference image information which is given by

$$\text{VIF} = \frac{I(\text{Test})}{I(\text{Reference})}$$

Where  $I(\text{Test})$  is the quantity of information extracted from the test image and  $I(\text{Reference})$  is the quantity of information extracted from a reference image. The higher the VIF index, higher the magnitude of test image. If VIF reaches to unity means that test image is perfect.

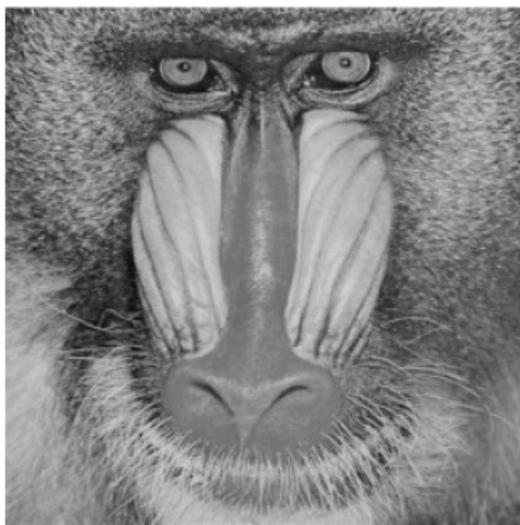
## 5. RESULTS AND ANALYSIS

The enhancing performance is tested using the images Lena, Elaine, Baboon, and Peppers and all simulations were carried out in MATLAB. Fig. 4 and Fig. 5 illustrates the low resolution test images and enhanced high resolution images respectively. In order to better perceive the difference in enhancing, enlarged segments of the images of Fig. 4 & 5 are shown in Fig. 6. The performance of the proposed method is analyzed by the variation of PSNR, BIQI Index, and VIF index of different images. Table 1, Table 2, and Table 3 give the performance comparison of the proposed and existing enhancing techniques in terms of PSNR, VIF, and BIQI index respectively. The results indicate that the proposed technique is better than the other methods in enhancing.

In this study, an efficient method is proposed for image resolution enhancement. The essence of the proposed work is the use of UDDWT for enhancement. The critically sampled discrete wavelet transform (DWT) have the drawbacks of shift variance, aliasing and lack of directionality. The DDWT is an improvement upon the critically sampled DWT and also nearly shift-invariant transform capturing directional information. Although the DDWT utilizes more wavelets, some lack a dominant spatial orientation, which prevents them from being able to isolate those directions. The UDDWT making the image exactly shift-invariant. The proposed method constructs a high resolution (HR) image from the given low resolution (LR) image by using forward and inverse UDDWT. The edge enhanced by using UDDWT. Future work may include enhancement of brightness by using Singular Value Decomposition (SVD).

Methods/ Images	Lena	Elaine	Baboon	Peppers
Bilinear	26.34	25.38	20.51	25.16
Bicubic	26.86	28.93	20.61	25.66
NEDI [1]	28.81	29.97	21.18	28.52
HMM [7]	28.86	30.51	21.47	29.58
DWT SR [8]	34.79	32.73	23.29	32.19
DWT & SWT SR [9]	34.82	35.01	23.87	33.06
SWT & LWT [10]	34.91	34.95	28.92	36.10
Proposed	40.32	42.78	34.06	39.76

TABLE 1: Comparison of PSNR in dB.



(a) BABOON



(b) ELAINE



(c) LENA



(d) PEPPERS

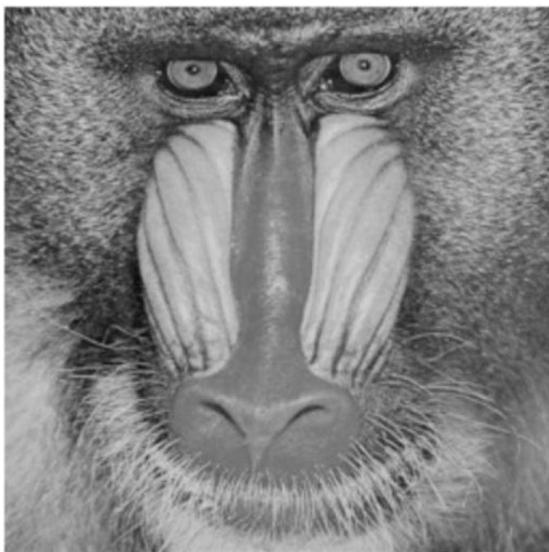
FIGURE 4: Low resolution test images.

Methods/ Images	Lena	Elaine	Baboon	Peppers
DWT & SWT SR [9]	0.14	0.19	0.17	0.19
SWT & LWT [10]	0.57	0.72	0.49	0.83
Proposed	0.67	0.71	0.51	0.85

**TABLE 2:** Comparison of VIF

Methods/ Images	Lena	Elaine	Baboon	Peppers
DWT & SWT SR [9]	28.21	34.02	46.09	34.37
SWT & LWT [10]	48.67	49.06	55.67	39.65
Proposed	51.24	52.85	58.43	43.42

**TABLE 3:** Comparison of BIQL.



(a) BABOON



(b) ELAINE



(c) LENA



(d) PEPPERS

**FIGURE 5:** Resolution Enhanced images.



**FIGURE 6:** Enlarged segments of the images of Fig. 4 & 5

## 6. CONCLUSION

The proposed method describes a new technique in image resolution enhancement. The technique enhances the resolution of the image by using Undecimated Discrete Wavelet Transform. The method uses a forward and inverse UDDWT to construct a high-resolution (HR) image from the given LR image. UDDWT also has nine sub bands similar to DDWT but sub bands in UDDWT are of same size of that of the image. The High Resolution image is reconstructed from the LR image using the inverse DDWT. This method is tested by using four well known images. The performance comparison shows that the proposed method is better than other enhancement methods.

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## Design of High Speed Low Power 15-4 Compressor Using Complementary Energy Path Adiabatic Logic

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### Abstract

This paper presents the implementation of a novel high speed low power 15-4 Compressor for high speed multiplication applications using single phase clocked quasi static adiabatic logic namely CEPAL (Complementary Energy Path Adiabatic Logic). The main advantage of this static adiabatic logic is the minimization of the  $1/2CV_{th}^2$  energy dissipation occurring every cycle in the multi-phase power-clocked adiabatic circuits. The proposed Compressor uses bit sliced architecture to exploit the parallelism in the computation of sum of 15 input bits by five full adders. The newly proposed Compressor is also centered around the design of a novel 5-3 Compressor that attempts to minimize the stage delays of a conventional 5-3 Compressor that is designed using single bit full adder and half adder architectures. Firstly, the performance characteristics of CEPAL 15-3 Compressor with 14 transistor and 10 transistor adder designs are compared against the conventional static CMOS logic counterpart to identify its adiabatic power advantage. The analyses are carried out using the industry standard Tanner EDA design environment using 250 nm technology libraries. The results prove that CEPAL 14T 15-4 Compressor is 68.11% power efficient, 75.31% faster over its static CMOS counterpart.

**Keywords:** Compressor; Static Adiabatic Logic, CEPAL (Complementary Energy Path Adiabatic Logic), Multi-phase Power-clocked Adiabatic Circuits .

---

### 1. INTRODUCTION

With the advancement in CMOS technology, chip capacity (transistor count) and clock frequencies have increased. As a result, the power dissipation of digital CMOS design has skyrocketed and now is a primary design constraint.[1] In the past, due to a high degree of process complexity and the exorbitant costs involved, low power circuit design was used in applications where very low power dissipation was absolutely essential, but now it became the norm for all high-performance applications.[2] So, low power techniques are highly appreciated in current VLSI design.

This has motivated the designers to explore various design approaches to reduce power dissipation in VLSI circuits. Adiabatic logic has been applied to low-power systems, and several adiabatic logic families have been proposed for low power applications [3]–[8]. Energy recovery circuits based on the adiabatic logic have been proved to be a promising approach among non-conventional low power design methodologies. The primary advantage of adiabatic circuits results

from its inherent nature of deriving a constant current from the appropriately called power-clock sources and making the FET switches function with minimum voltage across the source and drain [9].

There are several types of static adiabatic logic circuits, namely, Complementary Energy Path Adiabatic Logic (CEPAL), Quasi Static Energy Recovery Logic (QSERL) and Quasi Static Single-phase Energy Recovery Logic (QSSERL). They are all designed to overcome the drawbacks of the previously available irreversible adiabatic logic styles. These adiabatic circuits use sinusoidal power clock sources for operation. Since the sinusoidal power-clock generation has been proved versatile, it makes them suitable for energy recovery circuits as against the adiabatic logic styles employing trapezoidal or triangular power clock pulses.

Multiplication is the basic arithmetic operation in several microprocessors and digital signal processing applications. Digital Signal Processing systems require multipliers to implement DSP algorithms such as convolution and filtering where the multiplier lies directly within the critical path. Hence, the demand for high speed multipliers has become prominent. The enhanced speed leads to increased power dissipation, thus, power saving architectures turn to be the choice of the future. This has given way to the development of novel circuit techniques, with the aim of reducing the power dissipation of multipliers without compromising the speed and performance.

The earliest reported multiplier was an array multiplier that uses a chain of ripple carry adders to compute the product by means of repetitive addition [10]. Multiplier architecture is essentially divisible into three stages: a partial product generation stage, a partial product addition stage and final addition stage. A fast array or tree multiplier is composed of three sub-circuits: a Booth encoder for generation of partial products, a carry save structured accumulator for summing up the partial products and a final carry propagation adder to compute the final binary result from its stored carry representation [11]. The second stage requires the use of adders or Compressors and this stage mainly contribute to delay and power. Therefore speeding up the second stage and lowering its power dissipation are the most eminent means of achieving performance improvement of the multiplier. In high speed multipliers, 4-2 Compressors are widely used to lower the latency of the partial product accumulation stage. 4-2 compression is ideal for constructing regularly structured Wallace tree with low complexity. However, for the compression of a larger number of bits, higher orders Compressors are needed.

Section II gives an introduction to CEPAL. The proposed structure of 5-3 Compressor is given in Section III. The proposed structure of 15-4 Compressor and the details on how to implement it using CEPAL logic style is presented in the two subsequent sections. Experimental results are given in Section VI, and this paper is concluded in Section VII.

## 2. COMPLEMENTARY ENERGY PATH ADIABATIC LOGIC

The structure of the static energy recovery logic CEPAL is shown in Fig 1. CEPAL uses two complementary sinusoidal power clocks. The CEPAL consists of two transistors, Pull-up and Pull down networks charging and discharging transistors as seen in Fig. 1. Let us understand the operation of the circuit. Let us assume that the initial output  $V_{out}$  is high, and the Pull up network is on, while the Pull down network is off, the output node will neither be following the power clock PC nor its complement  $PC_{bar}$ , when the next input does not warrant a change in the output node.

Let us consider the alternate case, in which, the initial output  $V_{out}$  is low and the Pull up network is on, while the Pull down network is off. Then, the output node  $V_{out}$  follows either PC or its compliment  $PC_{bar}$ , whichever swings to high level. Once the output reaches high, it ramps down to low level following the power clock during its downward transition, thus making the node  $V_{out}$  to become a floating node. However, this condition is overcome when the compliment of the power clock swings to high level. This eliminates the weak high node and also eliminates the hold state of the two phase power clock operated circuits.

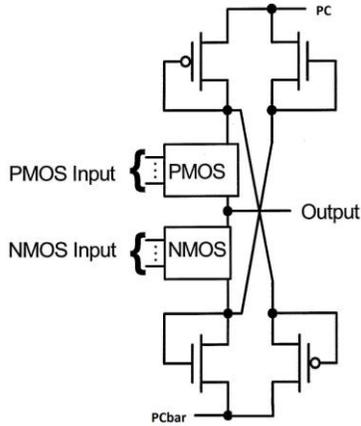


FIGURE 1: Complementary Energy Path Adiabatic Logic.

### 3. STRUCTURE AND DESIGN OF 5-3 COMPRESSOR

#### 3.1 Half adder

The half adder adds two single binary bits  $A$  and  $B$ . It has two outputs, sum ( $S$ ) and carry ( $C$ ). The input variables of a half adder are called the augend and addend bits. The carry signal represents an overflow into the next digit of a multi-digit addition. The simplest half-adder design incorporates an XOR gate for  $S$  and an AND gate for  $C$ . With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The structure of half adder is shown in the below figure.

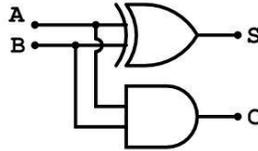


FIGURE 2: Logic Design of Half Adder.

The number of transistors and the average power of the Half Adder using CMOS and CEPAL are shown in Table 1.

Logic	P-MOS	N-MOS	Total Transistors	Average Power ( $\mu W$ )
CMOS	9	9	18	33.79
CEPAL	19	19	38	11.66

TABLE 1: Half Adder Transistor count & Power Comparison.

The CEPAL Half adder is 65.49% more power efficient as compared to its CMOS counterpart. Figure 3 shows the output waveforms of the CEPAL Half adder, where  $PC$  and  $PCbar$  are the two complementary power clocks. The plot  $p(VoltageSource\_4)$  shows the power dissipation of the power clock.



FIGURE3: Output waveforms of Half Adder.

### 3.2 Full adder

A full adder adds binary bits and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as  $A$ ,  $B$ , and  $C_{in}$ ;  $A$  and  $B$  are the operands, and  $C_{in}$  is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders. The circuit produces a two-bit output, that is, output carry and sum typically represented by the signals  $C_{out}$  and  $S$ . The structure of half adder is as shown in the below figure.

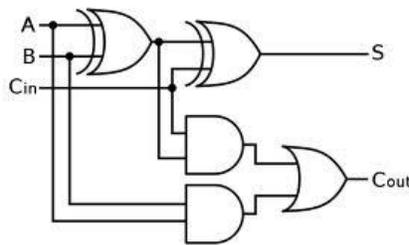


FIGURE 4: Logic Design of Full Adder.

The number of transistors and the average power of the Full Adder using CMOS and CEPAL are shown in Table 2.

Logic	P-MOS	N-MOS	Total Transistors	Average Power ( $\mu$ W)
CMOS	27	27	54	66.86
CEPAL	59	59	118	31.26

TABLE 2: Full Adder Transistor count & Power Comparison.

The CEPAL Full Adder is found to be 53.25% power efficient as compared to the counterpart in CMOS technology. Figure 5 shows the output waveforms of the CEPAL Full Adder. Plot PC and PCbar show the power clock given. The plot p(VoltageSource\_4) shows the power consumption of the power clock.



FIGURE 5: Output waveforms of Full Adder.

### 3.3 Architecture of 5-3 Compressor

A 5-3 Compressor comprises of a combinational logic circuit with five inputs and three outputs. It accepts a five bit input string, and produces its sum as output. The maximum output of a 5-3 Compressor can be 101, when all its input bits are at logic 1. The conventional architecture of a 5-3 Compressor is based on the design of a conventional 4-2 Compressor. The architecture of a conventional 5-3 Compressor is shown in figure 1.

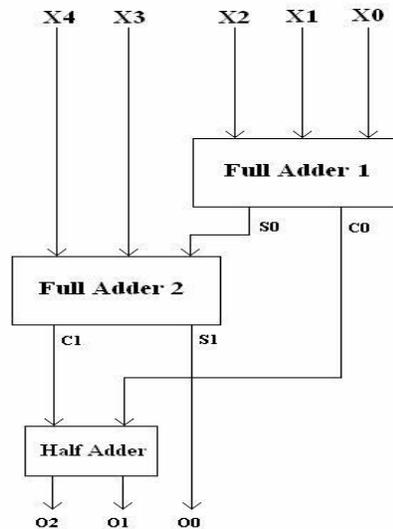


FIGURE 6: Architecture of conventional 5-3 Compressor.

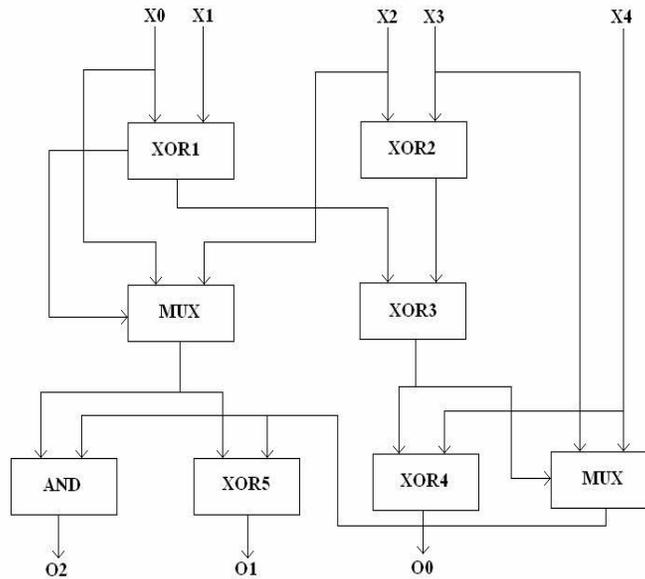
As evident from the figure 6, the implementation of the 5-3 Compressor has for 5 gate delays. Moreover the least significant bit of the output requires 4 gate delays (delay imposed by four XOR gates). As a result, there can be a problem of synchronization of the output bits when the input bits change leading to static hazards. We propose a novel architecture of a 5-3 Compressor that can produce output with only three gate delays. The architecture of the Compressor has been obtained by suitably rewriting the Boolean equations of a 5-3 Compressor as:

$$O_0 = x_0 \oplus x_1 \oplus x_2 \oplus x_3 \oplus x_4 \tag{1}$$

$$O_1 = ((x_0 \oplus x_1 \oplus x_2 \oplus x_3) \cdot x_4 \cdot \overline{(x_0 \oplus x_1 \oplus x_2 \oplus x_3) \cdot x_3}) \oplus ((x_0 \oplus x_1) \cdot x_2 + \overline{(x_0 \oplus x_1)} \cdot x_0) \tag{2}$$

$$O_2 = ((x_0 \oplus x_1 \oplus x_2 \oplus x_3) \cdot x_4 \cdot \overline{(x_0 \oplus x_1 \oplus x_2 \oplus x_3) \cdot x_3}) \cdot ((x_0 \oplus x_1) \cdot x_2 + \overline{(x_0 \oplus x_1)} \cdot x_0) \tag{3}$$

Using equations (1), (2) and (3), we propose to design a multiplexer based architecture of a 5-3 Compressor as shown in figure 7.



**FIGURE 7:** Architecture of proposed 5-3 Compressor.

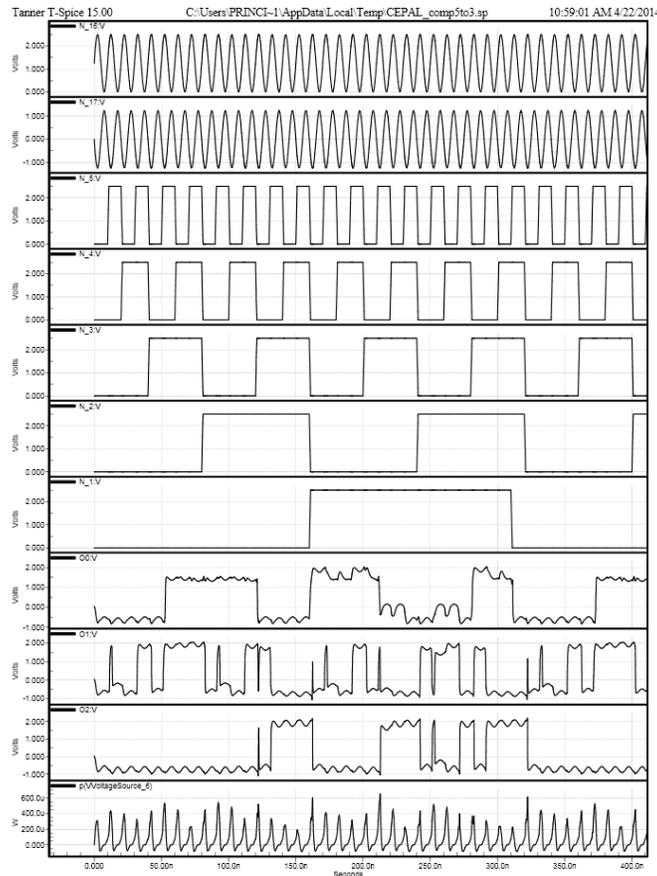
It is evident from Fig. 7, that the output of the Compressor requires 3 gate delays. It is therefore obvious that the proposed 5-3 Compressor computes the compressed output with a much lesser delay than the conventional 5-3 Compressor.

The number of transistors and the average power of the 5-3 Compressor using CMOS and CEPAL are shown in Table 3.

Logic	P-MOS	N-MOS	Total Transistors	Average Power ( $\mu$ W)
CMOS	45	45	90	74.64
CEPAL	91	91	182	41.84

**TABLE 3:** 5-3 Compressor Transistor count & Power Comparison.

There is an increase in the number of transistors in the CEPAL technology; nevertheless, there is a significant decrease in power. The CEPAL 5:3 Compressor is 43.94% more power efficient as compared to its CMOS counterpart. Figure 8 shows the output waveforms of the CEPAL 5:3 Compressor, where PC and PCbar are the two complementary power clocks. The plot p(VoltageSource\_10) shows the power dissipation of the power clock.

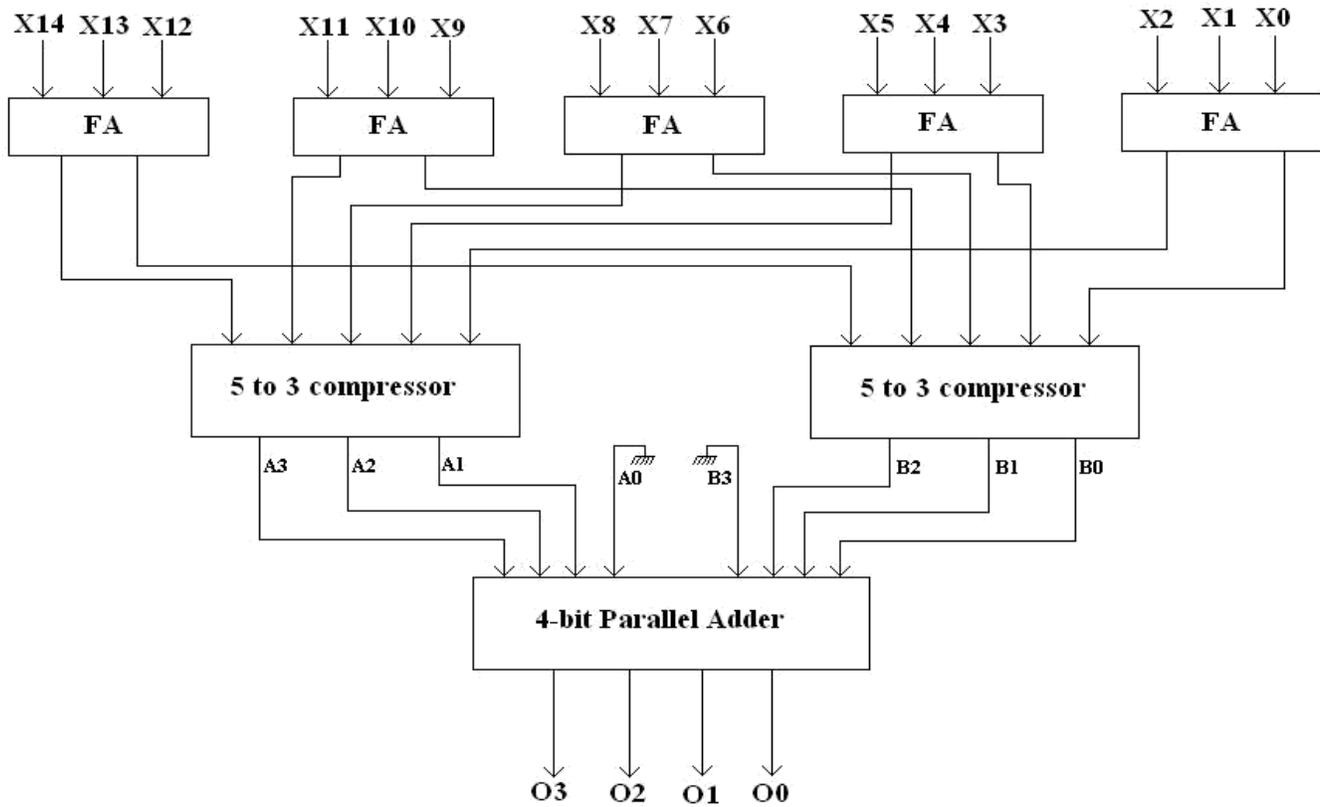


**FIGURE 8:** Output waveforms of proposed 5-3 Compressor.

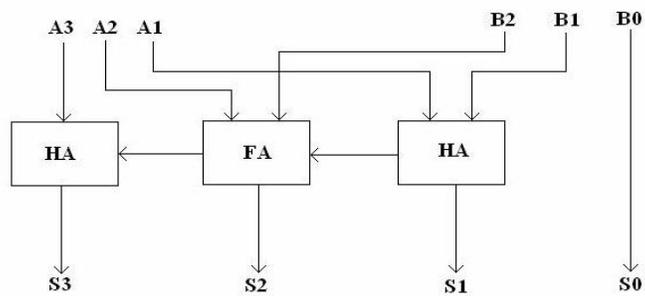
#### 4. ARCHITECTURE OF 15-4 COMPRESSOR

15-4 Compressor has been designed using the proposed 5-3 Compressor. The architectural design of the proposed 15-4 Compressor is shown in figure 9. The architecture is based on a bit sliced addition technique. The 15 input bits are divided five groups of three bits each. The 3 input bits in each group are compressed into 2 bits in the first stage using a full adder. The sum and carry outputs of each adder are thereafter sent to two 5-3 Compressors whose design has been discussed in section 3. The outputs of the Compressor are sent to a 4 bit parallel adder that has been suitably optimized according to the design requirements.

Since the 5-3 Compressor that computes the sum of the carry outputs of the full adders in the first stage produces a result that has twice the weight of the output of the other Compressor, hence the Compressor output is sent to the parallel adder after being appropriately left shifted. Since least significant bit of the one set of 4 bits is zero and the most significant bit of the other set of 4 bits is zero, hence the adder design is suitably optimized as shown in figure 10.



**FIGURE 9:** Architecture of proposed 15-4 Compressor.



**FIGURE 10:** Optimal design of Parallel adder.

## 5. CIRCUIT DESIGN OF 15-4 COMPRESSOR

The circuit has been designed, simulated and tested using 10 transistor [12] and 14 transistor [13] adder circuits. The design of the 10 transistor adder and 14 transistor adder are shown in figure 11(a) and 11(b) respectively.

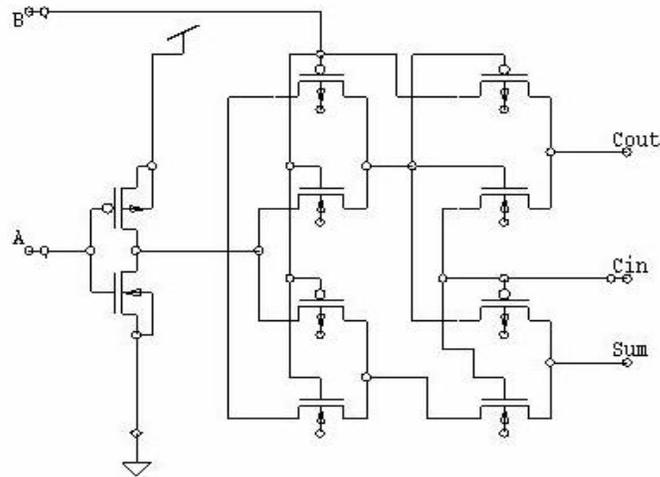


FIGURE 11 (a): Design of 10T adder.

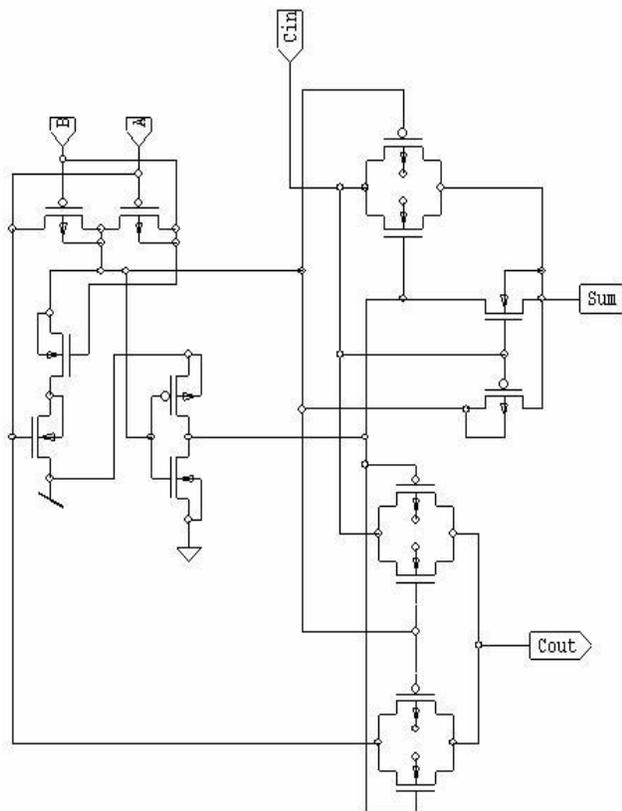


FIGURE 11 (b): Design of 14T adder.

## 6. RESULTS

The CEPAL (Complementary Energy Path Adiabatic Logic) based 15-4 Compressor is implemented using 250nm technology of the Tanner EDA with a W/L = 0.35 $\mu$ m/0.25 $\mu$ m and at 2.5V operating voltage along with a power clock frequency of 100MHz.

The number of transistors and the average power of the 15-4 Compressor using CMOS and CEPAL are shown in Table 4.

Logic	P-MOS	N-MOS	Total Transistors	Average Power ( $\mu$ W)	Delay (ps)	PDP (pJ)
CMOS based 10T adder design	160	160	320	261.14	549.67	0.144
CMOS based 14T adder design	170	170	340	349.17	536.31	0.187
CEPAL based 10T adder design	252	252	504	165.74	217.67	0.036
CEPAL based 14T adder design	262	262	524	111.35	135.70	0.015

**TABLE 4:** 15-4 Compressor Transistor count & Power Comparison.

The CEPAL 15-4 Compressor is found to be 68.11% power efficient, 75.31% faster as compared to its CMOS counterpart; this added advantage is a well worth tradeoff for the increased transistor count.

A comparative study of the simulation results presented in the above table indicates that the 14T adder based design is more efficient in terms of power, delay and power-delay product, although the circuit area becomes somewhat more compared to its 10T adder based counterpart.

## 7. CONCLUSION

In this paper, we have presented the implementation of 15-4 Compressor circuit using single phase adiabatic logic family, namely, CEPAL (Complementary Energy Path Adiabatic Logic). The CEPAL uses increased number of transistors than the CMOS logic style due to the necessity of using the MOS diodes, in the charging/discharging process paths. These MOS diodes used in the CEPAL structure makes it identified as a static logic and the use of diodes helps in reducing the switching activity. The CEPAL structure, being a static type of logic, incurs the reduced switching activity.

The newly proposed Compressor is also centered around the design of a novel 5-3 Compressor that attempts to minimize the stage delays of a conventional 5-3 Compressor that is designed using single bit full adder and half adder architectures. The proposed 15-4 Compressor uses the minimum number of hardware resources so far as the logic level architecture of the design is concerned.

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## Higher Order Feature Set For Underwater Noise Classification

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### Abstract

The development of intelligent systems for classification of underwater noise sources has been a field of research interest for decades. Such systems include the extraction of features from the received signals, followed by the application of suitable classification algorithms. Most of the existing feature extraction methods rely on the classical power spectral methods, which may fail to provide information pertaining to the deviations from linearity and Gaussianity of stochastic processes. Hence, many recent research efforts focus on higher order spectral methods in order to prevail over such limitations. This paper makes use of bispectrum, which is a higher order spectrum of order three, in order to extract a set of robust features for the classification of underwater noise sources. An SVM classifier is used for evaluating the performance of the feature set.

**Keywords:** Bispectrum, Bicoherence, SVM, HOS, Target Classification.

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### 1. INTRODUCTION

The development of intelligent systems for classifying underwater noise sources, based on their acoustic signatures has gained a considerable attention due to its strategic as well as commercial importance. Traditionally, power spectral analysis and its variants have been used as the feature extraction technique for such systems. However, being a linear method, and most of the complex signals like underwater noise are nonlinear, the use of power spectral analysis may turnout to be inadequate. Nonlinear methods may be used in such cases, in order to gain a more complete understanding of the underlying signal dynamics.

The bispectrum, which is based on the third order cumulant sequence of a signal, can play a key role in characterizing the nonlinearities of the underlying signal generating mechanisms, especially those containing quadratic nonlinearities [1]. Also, as bispectrum and all higher order spectra for Gaussian process are identically zero, it suppress the effect of additive white Gaussian noise while preserving the magnitude and phase information of the original signal. Bispectrum has been used in many signal processing applications, such as robust signal reconstruction [2], pattern recognition [3], [4] as well as detection of nonlinearities and quadratic phase couplings [1]. However, the direct use of bispectral or bicoherence matrix as a feature vector can pose the problem of high dimensionality. For example, when the direct method is used, with an  $N$  point FFT, the resulting matrix will have a dimension of  $N^2$  that is exponential in

nature, which for  $N = 128$  will account for 16384 data points, which obviously demands higher computational costs and even leads to over-fitting in certain cases.

Recent research efforts show a significant surge of interest in various types of integrated bispectra, due to its attractive properties of low dimensionality, scaling and translation invariance among others [3], [5]. The use of bispectrum estimate in detecting non-Gaussianity, nonlinearity, and harmonic coupling of underwater acoustic data has been demonstrated in [6]. Target classification attempts with bispectral features has been carried out in [7], [8] with a very limited number of targets. As it is obvious, a robust feature vector should capture the most invariant characteristics of the underlying signal, even in the presence of noise as well as in situations where the signal undergoes arbitrary scaling and translations that are quite common in underwater acoustic channels. This paper examines the feasibility of Integrated Bispectra, along with some other higher order features for deriving a robust feature set for underwater target detection and classification. The proposed algorithm has been evaluated using a database of 20 underwater targets in different levels of additive Gaussian noise.

The organization of the paper is as follows. Section 2 gives an overview of the higher order features. Feature selection is covered in section 3, and section 5 gives an overview of the SVM classifier. The details of the simulations conducted are presented in section 4. Finally, the results and discussions are given in sections 6 followed by the conclusions in section 7.

## 2. HIGHER ORDER FEATURE SET FOR CLASSIFICATION

Most of the existing feature extraction methods rely on the conventional power spectral estimation methods, which may fail to provide information pertaining to the deviations from linearity and Gaussianity of stochastic processes, as in the case of ocean acoustic signals. Such limitations motivate the use of higher order spectral methods instead of the conventional power spectral methods. Along with this, Bispectrum, being a higher order spectra of order three, is identically zero for many noise processes, especially the Gaussian process, it can be used to suppress the effect of additive white Gaussian noise while preserving the magnitude and phase information of the original signal [2]. The following sections describe the higher order features used in this paper.

### 2.1 Bicoherence

The third order spectrum or the bispectrum  $B(f_1, f_2)$  is defined as the Fourier transform of the third order cumulant.

$$\begin{aligned} B(f_1, f_2) &= \sum_{k=-\infty}^{\infty} \sum_{l=-\infty}^{\infty} C_{xx}(k, l) \exp(-j2\pi f_1 k) \exp(-j2\pi f_2 l) \\ &= E\{X(f_1)X(f_2)X^*(f_1 + f_2)\} \end{aligned} \quad (1)$$

It is found that, at the bifrequency  $(f_1, f_2)$ , the complex variance of the bispectrum is proportional to the product of the power of the signals [9] at the frequencies  $f_1, f_2$  and  $(f_1 + f_2)$ . That is,

$$\text{var}[B(f_1, f_2)] \propto P(f_1)P(f_2)P(f_1 + f_2) \quad (2)$$

Thus, in order to make the bispectrum independent of the energy content at the bifrequencies, another parameter called bicoherence is used. Bicoherence, which is a normalized form of the bispectrum, can be defined as [1],

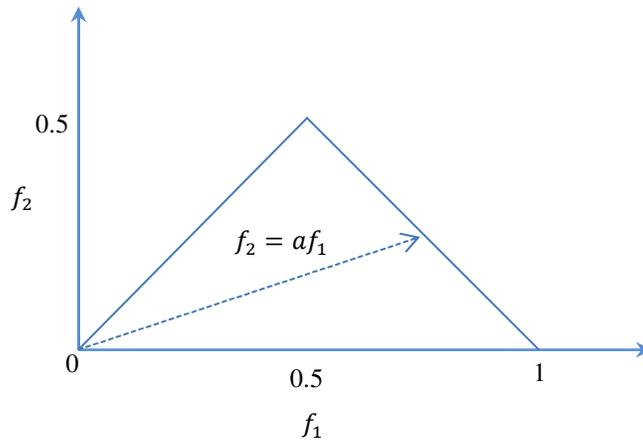
$$\text{bic}(f_1, f_2) = \frac{|B(f_1, f_2)|}{[P(f_1)P(f_2)P(f_1 + f_2)]^{1/2}} \quad (3)$$

Since the bicoherence is independent of the energy or amplitude of the signal, it can be used as a convenient test statistic for the detection of non-Gaussian, non-linear and coupled processes. Here, the diagonal and anti-diagonal slices of the bicoherence matrix have been used as the feature vector.

**2.2 Radially Integrated Bispectrum (RIB)**

Chandran and Elgar [3], first proposed the use of radially integrated bispectra in pattern recognition and demonstrated its applicability. The RIB is obtained by integrating the bispectrum along radial lines passing through the origin in bifrequency space, as shown in Figure 1. The integrated bispectra can be defined as:

$$RB(a) = \int_{0+}^{1/(1+a)} B(f_1, af_1)df_1 \tag{4}$$



**FIGURE 1:** RIB Computation - Integrating the bispectrum along the dashed line with slope=a.

In the discrete domain, the integration can be approximated by

$$RIB(a) = \sum_{k=1}^{\lfloor (\frac{N}{2}-1)/(1+a) \rfloor} B(f_1, af_1) \tag{5}$$

**2.3 Circularly Integrated Bispectrum (CIB)**

As the name suggests, for the Circularly Integrated Bispectrum, the integral paths are a set of concentric circles with the origin as the center. The CIB can be defined as [10]:

$$CIB(a) = \int B_p(a, \theta)d\theta \tag{6}$$

where  $B_p(a, \theta)$  is the polar representation of  $B(\omega_1, \omega_2)$

**2.4 Axially Integrated Bispectrum (AIB)**

The Axially Integrated Bispectrum (AIB) is obtained by integrating the bispectra along paths parallel to the  $\omega_1$  or  $\omega_2$  axes in bifrequency plane and retains the scale characteristics of the signal [11].

$$\begin{aligned}
 AIB(\omega) &= \frac{1}{2\pi} \int_{-\infty}^{\infty} B(\omega_1, \omega_2) d\omega_2 \\
 &= \frac{1}{2\pi} \int_{-\infty}^{\infty} B(\omega_1, \omega_2) d\omega_1
 \end{aligned} \tag{7}$$

Though the AIB contains less phase information when compared to the bispectra, the estimation variance of the AIB is much less, equivalent to that of power spectrum.

### 2.5 Bispectral-MFCC (BMFCC)

The Mel Frequency Cepstral Coefficients (MFCC) has been widely used in various feature extraction scenarios due to its low computational complexity and good performance under clean matched conditions. However, the performance of MFCC is directly proportional to the Signal to Noise Ratio (SNR), hence the performance generally degrades rapidly in the presence of noise [12].

Since the bispectrum suppress the additive white Gaussian noise while preserving the magnitude and phase information of the original signal, it can be used to compute a clean estimate of the magnitude spectrum of the noisy signal. The estimated spectral magnitude  $|X(\omega)|$  is obtained as:

$$|X(\omega)| = e^{[DFT(g(n))]} \tag{8}$$

where,

$$g(n) = F_1^{-1} \left[ \frac{1}{2\pi} \int_{-\pi}^{\pi} \log(|B(\omega_1, \omega_2)|) d\omega_2 \right] \tag{9}$$

The final BMFCC features has been computed from the estimated spectrum  $|X(\omega)|$  by adopting the usual MFCC feature extraction method. The block diagram illustrating the steps of the BMFCC extraction is given in Figure 2.

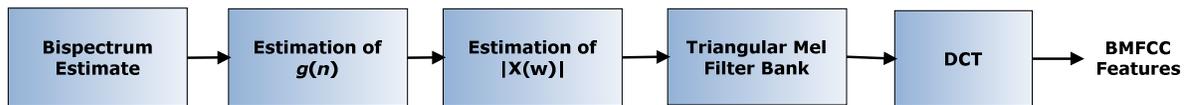


FIGURE 2: BMFCC Feature Extraction.

## 3. FEATURE SELECTION

High dimensional feature space can pose problems like over-fitting to trivial aspects of the signal and high computational burdens. Therefore it would be desirable to identify a salient subspace of the original feature space based on some decision criteria, that would effectively remove the irrelevant or redundant features while leaving out the most discriminant ones intact, and the process is generally termed as feature selection.

### 3.1 Fisher Ratio for Class Separability Measure

The Fisher Ratio depends on the interclass difference and the intraclass spread or variance, and is defined as the ratio of the interclass difference to the intraclass spread [13]. Let the mean and variance of the  $l^{th}$  feature of the classes  $C_i$  and  $C_j$  are denoted by  $m_{i,l}$ ,  $m_{j,l}$ ,  $\sigma_{i,l}^2$  and  $\sigma_{j,l}^2$  respectively.

The Fisher Ratio of the  $l^{th}$  feature is then defined as

$$\lambda_{i,j,l} = \frac{(m_{i,l} - m_{j,l})^2}{(\sigma_{i,l}^2 + \sigma_{j,l}^2)} \tag{10}$$

The definition given in equation (10) can be further extended to multiclass problems, where there are  $C$  classes, in order to find the average class separability measure  $\lambda_l$  of the  $l^{th}$  feature,

$$\lambda_l = \frac{\sum_{i=1}^C \sum_{j=1}^C \lambda_{i,j,l}}{C(C-1)}, \quad i \neq j \quad (11)$$

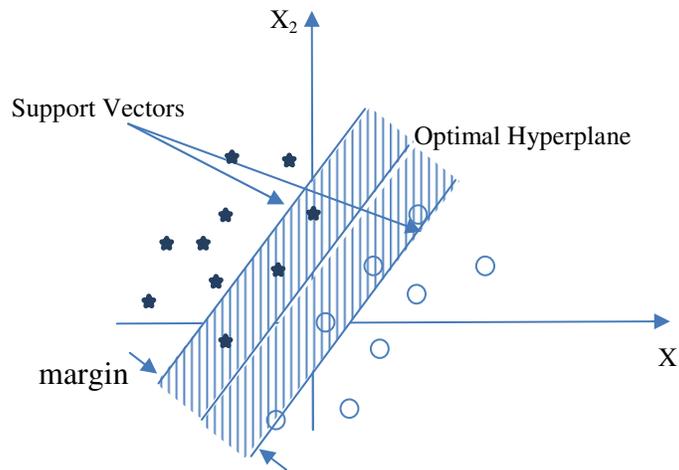
A high value of  $\lambda$  indicates less intraclass spread and more interclass difference, hence represents a strong discriminative feature. Feature selection has been accomplished by retaining all features having a  $\lambda$  value above a predetermined threshold.

#### 4. SVM CLASSIFIER

The theory behind SVM relies on the fact that it is possible to transform the data into a space where the classes are linearly separable with dimensionality at least equal to the data's Vapnik-Chervonenkis (VC) dimension [14]. That is, some nonlinear operator  $\Phi(\circ)$  is used to map the input pattern  $x$  into a higher dimensional space  $H$  so that the transformed data is linear in  $H$ . In general a kernel function  $K(\circ, \circ)$  which implicitly defines the nonlinear mapping function  $\Phi(\circ)$  can be used to map the nonlinear space into a linear one. There are a wide variety of possible Kernel functions, including linear, polynomials and RBFs. In this paper, an RBF Kernel has been used, which is defined as:

$$k(x_i, x) = e^{-\|x-x_i\|^2 / (2\sigma^2)} \quad (12)$$

For any kernel, there will be some parameters that would determine the properties and efficiency of the classifier involved. For instance, there are two parameters for an RBF kernel, namely  $C$  and  $\gamma$ . The optimal values for these parameters are not known beforehand and consequently some kind of model selection (parameter search) must be carried out in order to ensure the best possible performance of the classifier. Cross-validation and Grid-search is an efficient and simple strategy for identifying such optimal values for the kernel parameters [15]. Once the data has been transformed to the higher dimensional space  $H$ , there may exist many hyperplanes that separate the classes as shown in Figure 3.



**FIGURE 3:** Hyper plane and support vectors.

The SVM classifier will try to find the hyperplane that maximizes the separating margin between two classes and this can be further extended to multiclass scenarios [16].

## 5. DETAILS OF EVALUATIONS CONDUCTED

A set of acoustic waveforms collected from 20 underwater noise sources has been used for evaluation of the system. Each of these noise waveforms is sliced in to 20 frames of 10240 elements, with a finite overlapping. The bispectrum and bicoherence matrix of each record is computed using equation (1) and equation (3). The following features were extracted from the target waveforms

- a) Axially Integrated Bispectra (AIB)
- b) Radially Integrated Bispectra (RIB)
- c) Circularly Integrated Bispectra (CIB)
- d) Bispectral-MFCC (BMFCC)
- e) Diagonal and anti-diagonal slice of the bicoherence matrix (DiagBic)

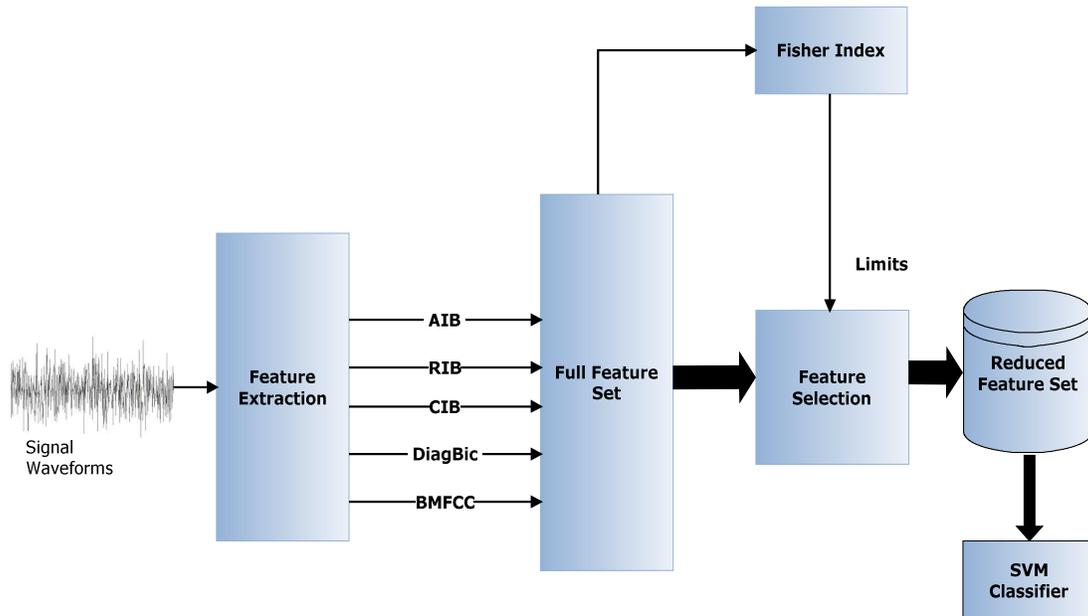
No.	Feature	Properties	Ref.
(a)	Axially Integrated Bispectra (AIB)	Translation invariance	[11]
(b)	Radially Integrated Bispectra (RIB)	Scale invariance	[3]
(c)	Circularly Integrated Bispectra (CIB)	Translation invariance	[10]
(d)	Bispectral-MFCC (BMFCC)	Noise resistance, as it is derived from Bispectrum	[12]
(e)	Diagonal and anti-diagonal slice of the bicoherence matrix (DiagBic)	Self coupling Frequencies	[1]

A subset of the original feature set containing only relevant features that would potentially contribute to the classification process has been computed using equation (11), considering all targets. Simulations were conducted with different limits for the fisher's score, for each feature. From these simulations, an optimal threshold for each feature was identified. Table 1 summarises the thresholds and the percentage of the features selected during feature selection.

Feature Vector	Threshold	%of Features Used
RIB	600.00	58.24
CIB	2500.00	51.56
AIB	1000.00	60.94
BMFCC	1000.00	46.00
DiagBic	250.00	30.86
<b>Overall</b>		<b>45.16</b>

**TABLE 1:** Result of feature selection using Fisher's Criterion.

The reduced feature sets has been combined to train an SVM classifier. The whole procedure is illustrated in the Figure 4. A Matlab based framework has been developed in order to evaluate the performance of the proposed classifier system under realistic scenarios. Since the underwater acoustic signals are generally corrupted by the ambient noise which is Gaussian in nature, the framework provides options for adding white Gaussian noise to the signals to ensure the robustness of the classifier in the presence of noise. Simulations were also carried out to study the performance of SVMs trained with different noise levels.



**FIGURE 4:** Block diagram of the complete training Process.

## 6. RESULTS AND DISCUSSIONS

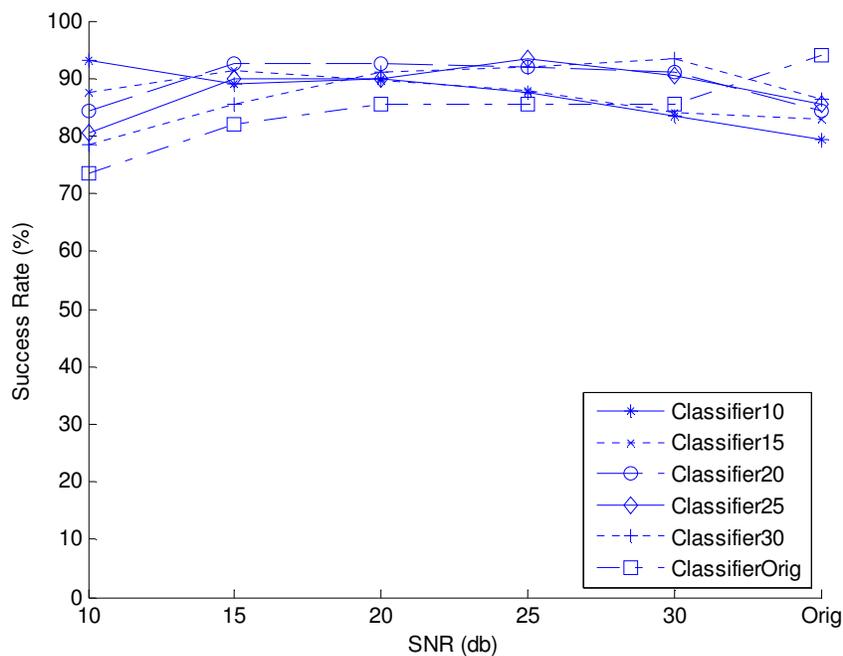
The noise data used for evaluating the performance of the classifier mainly comprises of anthropogenic noises as well as biological noises. Some of the data sets used in developing the database were collected during scheduled cruises off Cochin and Mangalore, India. For the purpose of validating the performance of the classifiers, 400 records from 20 different targets were considered. White Gaussian noise were added to the waveforms to synthesize signals with different SNRs of 10, 15, 20, 25 and 30 db, and corresponding feature sets were extracted.

A total of 6 SVMs, each trained with different noise levels (10, 15, 20, 25,30 db and the original signal) were used for the analysis. The performance of each SVM was evaluated with all feature sets corresponding to different noise levels. In each case, an SVM classifier was trained with a training set comprising 200 randomly selected records and the success rate of the classification was evaluated. The analysis was performed 5 times, with randomly selected training set and the average performance was computed in order to get statistically reliable results.

The results of the analysis has been summarized in Table 2. Here, Classifier $N$  represents a classifier trained with the features extracted from signals with white Gaussian nose added, so that the SNR is  $N$  db. For example, a success rate of 92.50% has been obtained when the SVM trained on a feature set extracted from signals having SNR of 20db, evaluated with features corresponding to 15db SNR. Classifier $Orig$  denotes the classifier trained with the original signal, without adding any noise. A plot of the success rates of different classifiers is illustrated in Figure 5.

	SNR (db) of the evaluation set						Average
	10	15	20	25	30	Original Signal	
Classifier10	93.00	89.00	90.00	87.50	83.50	79.50	87.08
Classifier15	87.50	91.50	89.50	88.00	84.00	83.00	87.25
Classifier20	84.50	92.50	92.50	92.00	91.00	84.50	89.50
Classifier25	80.50	90.00	90.00	93.50	90.50	85.50	88.33
Classifier30	78.50	85.50	91.00	92.00	93.50	86.50	87.83
ClassifierOrig	73.50	82.00	85.50	85.50	85.50	94.00	84.33

**TABLE 2:** Success rate of SVM classifiers.

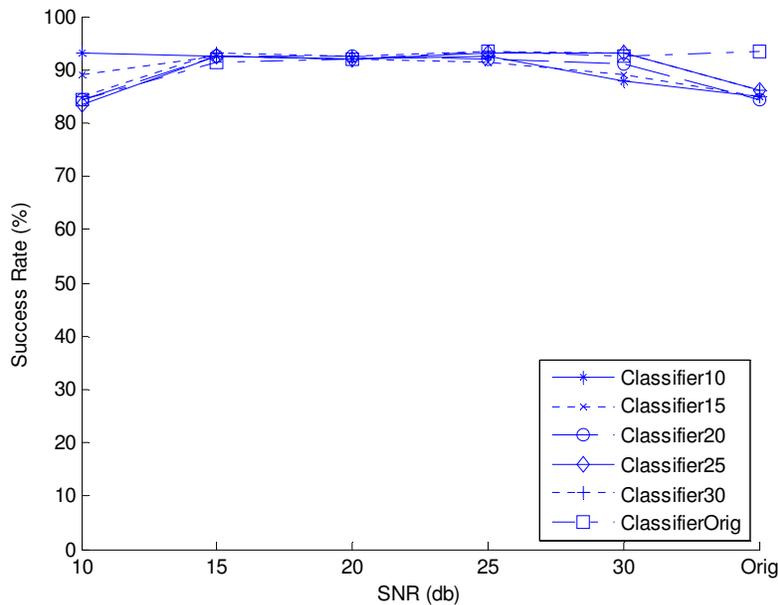


**FIGURE 5:** Plot showing the success rate of different classifiers.

From the simulations carried out, it was concluded that classifiers trained with signals of 20db SNR perform reasonably well for other situations of noises as well. So finally, the training sets of all individual classifiers were expanded to include features corresponding to 20db SNR and the simulation results are summarized in Table 3. Clearly, there is an improvement in success rate, which can be easily verified from the improvements in the average success rate of each classifier. The results are also illustrated graphically in Figure 6.

	SNR (db) of the evaluation set						Average
	10	15	20	25	30	Original Signal	
Classifier10	93.00	92.50	92.00	92.50	88.00	85.00	90.50
Classifier15	89.00	92.50	92.00	91.50	89.00	85.00	89.83
Classifier20	84.50	92.50	92.50	92.00	91.00	84.50	89.50
Classifier25	83.50	92.50	92.00	93.00	93.00	86.00	90.00
Classifier30	85.00	93.00	92.50	93.50	93.00	86.00	90.50
ClassifierOrig	84.50	91.50	92.00	93.50	92.50	93.50	91.25

**TABLE 3:** Success rate of classifiers with expanded training set.



**FIGURE 6:** Plot showing the improved success rate.

## 7. CONCLUSIONS

A set of robust features derived from bispectral analysis has been proposed for underwater noise classification. The features include three types of integrated bispectras along with bispectral MFCC coefficients and self-coupling frequencies. A feature selection algorithm is used to select a robust subset of the features and an SVM classifier has been used to evaluate the classification performance. From the simulations conducted, it has been observed that the proposed higher order feature set could potentially improve the overall success rate of the classification of underwater noise sources even in the presence of different levels of ambient noise. The future work may include the incorporation of higher dimensional feature sets like trispectrum along with more robust feature selection algorithms.

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