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EDITORIAL PREFACE

This is the *Second* Issue of Volume *Thirteen* for International Journal of Engineering (IJE). The Journal is published bi-monthly, with papers being peer reviewed to high international standards. The International Journal of Engineering is not limited to a specific aspect of engineering but it is devoted to the publication of high quality papers on all division of engineering in general. IJE intends to disseminate knowledge in the various disciplines of the engineering field from theoretical, practical and analytical research to physical implications and theoretical or quantitative discussion intended for academic and industrial progress. In order to position IJE as one of the good journal on engineering sciences, a group of highly valuable scholars are serving on the editorial board. The International Editorial Board ensures that significant developments in engineering from around the world are reflected in the Journal. Some important topics covers by journal are nuclear engineering, mechanical engineering, computer engineering, electrical engineering, civil & structural engineering etc.

The initial efforts helped to shape the editorial policy and to sharpen the focus of the journal. Started with Volume 13, 2021, IJE will be appearing with more focused issues. Besides normal publications, IJE intend to organized special issues on more focused topics. Each special issue will have a designated editor (editors) – either member of the editorial board or another recognized specialist in the respective field.

The coverage of the journal includes all new theoretical and experimental findings in the fields of engineering which enhance the knowledge of scientist, industrials, researchers and all those persons who are coupled with engineering field. IJE objective is to publish articles that are not only technically proficient but also contains information and ideas of fresh interest for International readership. IJE aims to handle submissions courteously and promptly. IJE objectives are to promote and extend the use of all methods in the principal disciplines of Engineering.

IJE editors understand that how much it is important for authors and researchers to have their work published with a minimum delay after submission of their papers. They also strongly believe that the direct communication between the editors and authors are important for the welfare, quality and wellbeing of the Journal and its readers. Therefore, all activities from paper submission to paper publication are controlled through electronic systems that include electronic submission, editorial panel and review system that ensures rapid decision with least delays in the publication processes.

To build its international reputation, we are disseminating the publication information through Google Books, Google Scholar, J-Gate, ScientificCommons, Docstoc and many more. Our International Editors are working on establishing ISI listing and a good impact factor for IJE. We would like to remind you that the success of our journal depends directly on the number of quality articles submitted for review. Accordingly, we would like to request your participation by submitting quality manuscripts for review and encouraging your colleagues to submit quality manuscripts for review. One of the great benefits we can provide to our prospective authors is the mentoring nature of our review process. IJE provides authors with high quality, helpful reviews that are shaped to assist authors in improving their manuscripts.

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FETs as a Congruous Hardware in Embedded Technology and Sensors

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Abstract

VLSI FET technology is taking leaps and bounds in deciding the future of embedded technology. Newest technologies based on number of gates, FET arrangement, type of materials which have been presented lately are analyzed and its beneficiaries and deficiencies are pointed out. These new categories of materials include transistors manufactured from Silicon (Si), Germanium (Ge), Gallium Arsenide (GaAs), and Indium Gallium Arsenide (InGaAs), organic materials. Various considerations are shortlisted before deciding the ideal FET technology and the benchmarks. These benchmarks describe the properties and parameters which are necessary for deciding the FET technology. Palpable factors include availability of material, switching speed, ease of manufacturing, power dissipation, hardware complexity, thickness, band gap, threshold voltage, mobility of charge carriers, efficiency, scaling factors, etc. Detailed discoveries of the specifications are stated including summaries, graphical comparisons and suggestions of the type of hardware which is judicious are discussed. Such a technology will be useful for embedded processors and sensors. When manufactured, it will be a beneficial hardware for deep learning and machine learning algorithms and its application.

Keywords: FET Arrangement, Technologies, Benchmarks, Materials, Applications.

1. INTRODUCTION

Field Effect Transistor (FET) is a device which mainly contains 3 main terminals. A source and drain through which current conduction and electron transfer takes place. A gate through which voltage is injected into the transistor such that the conduction takes place. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the commonly used FET which is the backbone of Very Large Scale Integrated (VLSI) products. FET is the foundation to almost every electronic product. This makes it an essential factor in designing a product.

Technology and advancements in FETs have resulted in giving rise to various types of FET. Certain FETs are application based and others are general purpose ones. The advancements in this technology have made it a hard decision of which FET design should be utilized. Many performance characteristics and statistics must be analyzed before a decision. Even availability of the type of FET and the cost plays a big role. In this scenario a swift decision needs to be taken in selecting the type of hardware material and design, so that products can be efficiently and quickly manufactured.

In the last decade, the applications of the FET technology were limited to a certain market. With the rise of RISC and CISC machines and development of fast embedded products, the software codes and algorithms have hit a barrier as to how quick a device needs to perform. To analyze complex machine learning algorithms and deep learning algorithms, chip processing rate and the clock speed must improve constantly with time to prevent a bottleneck. Consequently, research in the form of effort and funds have been put in by different electronic design companies and manufacturers to provide the best quality hardware support and optimal performance.

Designing a hardware not only requires performance, but also many other factors must be kept in mind before deciding which type of hardware should be manufactured. Safety factors, environmental concerns, and fault diagnostics should be considered as well. Section 2 of this paper provides information of certain ways in which FETs are designed and the arrangement are described [1][2][3][4]. Section 3 contains important information describing and evaluating the performance criteria mentioned in [5] [6] and [7]. We have summarized a few existing FET technologies which have been abundantly used and classified them based on certain factors to conclude which technology can yield a sizeable result in the embedded processors and make use of the artificial intelligence in a beneficial way in Sections 4, 5, 6 and 7.

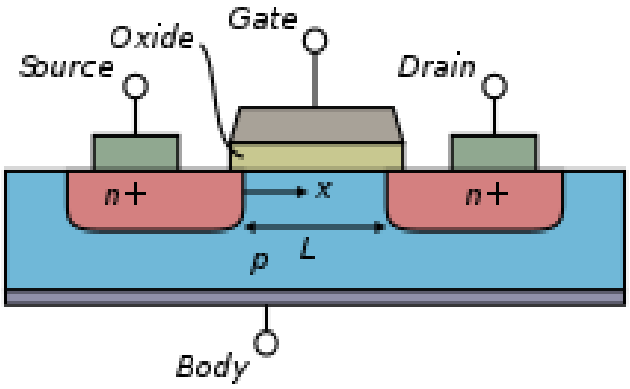

FIGURE 1: N-type MOSFET [5].

2. CLASSIFICATION OF FET TECHNOLOGY

FET technology can be classified in many ways depending upon the number of gates, arrangements, and composition. The main categories include:

2.1 Technology based on Number of Gates

FET is manufactured generally by using an insulating material to which Gate is attached. The voltage at Gate controls the flow of electrons and hence decides the amount of current (electrons) flow through the channel from source to drain. Gate is generally in the form of metal contacts and the number of metal contacts is based on the number of Gates in the FET. In this manner, the FETs can be classified as:

1. Single Gate
2. Double Gate
3. Tri Gate
4. Gate All Around (GAA)

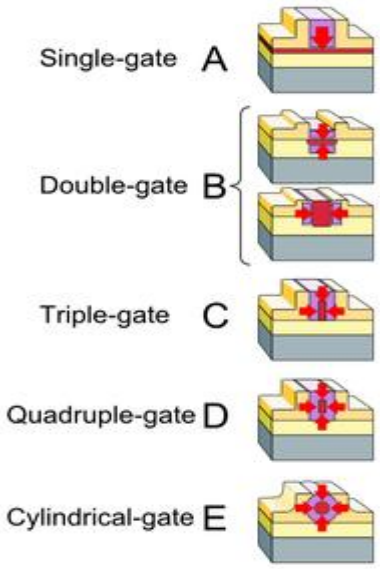

FIGURE 2: Different Gate Configuration [3].

1. Single Gate: In a Single Gate FET, there is a semiconductor layer above a layer of dielectric material. The dielectric layer is generally referred to as Buried OXide (BOX) and the Gate OXide (GOX). There is a p-type layer in between the BOX and the GOX, which prevents any entry of depletion region into the p-type substrate. There are two types of FETs namely partially depleted FET and fully depleted FET.

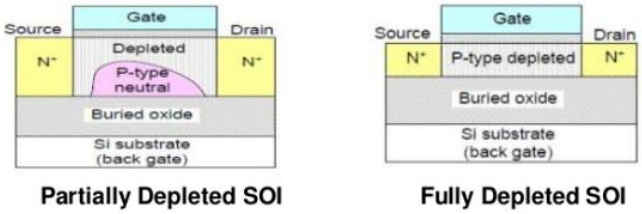

FIGURE 3: Partially Depleted (PD) SOI and Fully Depleted (FD) SOI [10].

It is easier to construct a PD SOI whereas FD SOI utilizes the total film of the depletion region. FD SOI has approximately 22% faster data transfer and in small transistors where Gate length is less than 50 nm, there is very quick switching speed. FD SOI is preferred and is mandatory for the manufacturing of the other types of Gate FETs. Single FETs find their use in switches, calculators, amplifiers, multiplexers, etc.

2. Double Gate FET (DGFET): Single Gate FETs do not have a conducting plane at the bottom of the semiconductor region as it has a very thin film. To overcome this problem double Gate FETs were introduced. Moore's law states that "The number of transistors on a chip doubles every two years while the costs are halved". When the transistor technology moved into the 21st century era, DGFET played an important role in making sure that Moore's law stands true. This helped in making FETs whose size is in the range from 20nm to 50nm. A DGFET has a thin semiconductor channel controlled by the metal gates on two sides. The buried oxide layer thickness is diminished considerably such that the ground plane gets connected to one of the Gates. In this case, the top gate acts as a conventional single Gate FET and the ground plane acts as a bottom Gate. Switching can be carried out using both gates simultaneously or by applying bias to one of the Gates. The types of DGFET includes planar (horizontal Gate or channel), vertical direction of conduction and FinFET (vertical channel and parallel conduction).

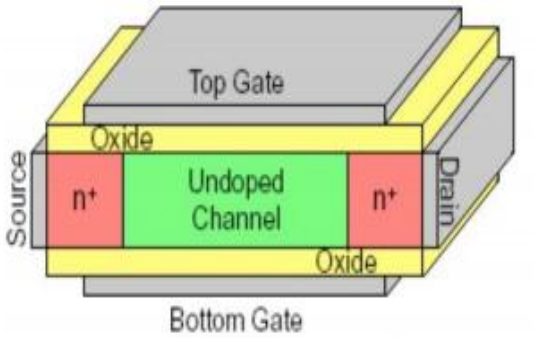

FIGURE 4: Double Gate FET (DGFET) [2].

Despite DGFET being a complex and costly technology as compared to single Gate FETs, it has pros such as having better switching time, good mobility of carriers, less leakage of current, and power thus giving high efficiency for low power consumption. The new Complementary Instruction Set Computing (CISC) chips manufactured by Intel (SkyLake), AMD (Ryzen) are generally a FinFET which is a type of DGFET technology.

3. Tri Gate FET: While manufacturing a FinFET, an aspect ratio which is the ratio of the width, and the height of the semiconducting material needs to be greater than 1. Such construction requires huge doping to prevent leakage between the Source and the Drain regions. A tri-Gate FET has a Gate present on top of the two Gates as shown in Fig. 2, which provides a square or a rectangular cross section by helping to reduce the travelling distance of the electrons considerably as compared to FinFET. Intel studies reflect that the minimization of electron travel distance is approximately 3 times and a huge reduction in leakage current and power.

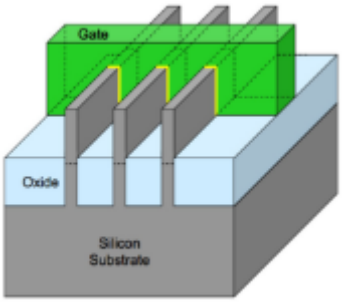

FIGURE 5: Tri-Gate FET [2].

There is less deviation of threshold voltage with respect to channel width in tri-Gate MOSFET as compared to DGFET. The performance of tri-Gate can be improved by using Pi- Gate and Omega Gate. This is basically increasing the walls of the GOX. Tri-Gate MOSFETs are used in making carbon nanotubes, ICs, memory chips, and processors.

4**.** Gate All Around (GAA): Gate All Around means the gate is enveloping the channel from all the sides. It provides effective coupling between the capacitors of the Gate and the channel. Thus, resulting in low channel noise and high on-off ratio in addition to the improved carrier transport. Generally, all GAAs are made of Germanium rather than silicon. Samsung and Intel suggest experiments that when channel width is reduced to less than 5nm, there is trouble in handling a FinFET or a tri-gate. Specific research in GAA FETs suggests that these FETs are the one for the future when smaller chip sizes with extra performance will be required.

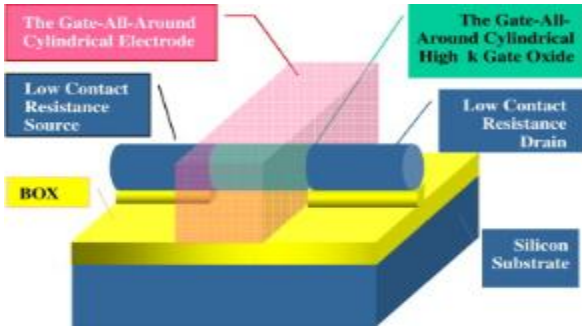

FIGURE 6: Gate All Around FET [2].

2.2 Technology based on Arrangement of FETs

Integrated Circuit design is fabricated using technologies like planar (2D structure) and non-planar (3D structure) technologies.

1. Planar FET: It has a two-dimensional arrangement, where the channel is positioned between source and drain region and Gate electrode is positioned above the channel. Examples of Planar FETs include N-type MOSFET and P-type MOSFET. Applications of these FETs are in integrated circuits such as microprocessors and memory devices which provides switching functions for logic gates and in data storage. Manufacturers of planar MOSFETs include Texas Instruments, STMicroelectronics, and Infineon, etc.

Since conventional planar bulk silicon MOSFET scaling started slowing down. The non-planar device structures become inevitable in continuation of performance improvement. It is seen as a cost-effective way by most major manufacturers to maintain the progress than to invest with completely new technologies.

2. Non-Planar FET: In contrast to planar structure, a non-planar has a three-dimensional structure. It has a vertically raised, fin-shaped source and drain regions where the gate is positioned on two, three, or four sides of the channel or wrapped around the channel, forming a double gate or multigate structure. These devices are given a generic name “FinFETs or MuGFETs” because the source/drain region forms fins on the silicon surface**.**

Companies using this technology are AMD, NVidia, IBM, ARM, Motorola and Intel. Non-planar has faster switching times and higher current density than planar structures.

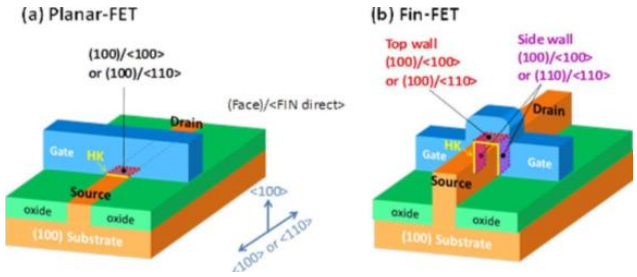

FIGURE 7: Planar FET and Non-planar FET [3].

2.3 Classification of FETs based on composition

FETs are generally transistors whose main function is transferring electrons and carry from source to drain for conduction of current. The ideal material for having this conduction are semiconducting materials which are generally neutral, making charge transfer in both directions relatively simple. Common semiconducting materials used are silicon carbide (SiC), gallium

arsenide (GaAs), gallium nitride (GaN), and indium gallium arsenide (InGaAs). There are some FETs which act like sensors as well.

1. Silicon (Si)**:** It is one of the most abundant materials on the surface of the earth as it is a component of sand. This makes it a comfortable and convenient choice for early engineers and researchers working in the transistor field to select this material as the main component for FET. It has suitable electrical properties such as a wide bandgap (which prevents current leakage and power draining), it also has good thermal conductivity (maintaining appropriate temperature of the circuits even after draining a huge amount of power). To manufacture IC's and electronic hardware, wafers need to be built in laboratories. A lot of investment must be made so that the labs can produce the demand of wafers which are needed to make the hardware electronics. This investment has already been made by Marquiz companies such as Intel, Texas Instruments, Silicon Labs, Toshiba, Micron, and NXP Semiconductors who have already built and made huge investments in making silicon as the primary component for these wafers.

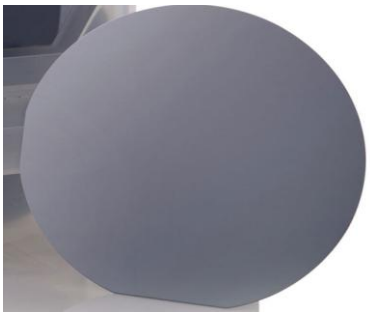

FIGURE 8: Silicon Wafers [5].

2. Germanium (Ge): Germanium which is like Silicon, is a semiconducting material used as a primary material in FET. Research on Ge FETs were called off during the early stages as Silicon had a larger band gap and was far more abundant in nature. Current research suggests that Germanium can provide high performance than Silicon due to its superior mobility of electrons and holes. The newer FETs need to improve in performance with increased density and therefore Germanium can be a substitute to Silicon in newer generations of FETs. IBM supercomputers are the gifts of Germanium based nanowire FETs.

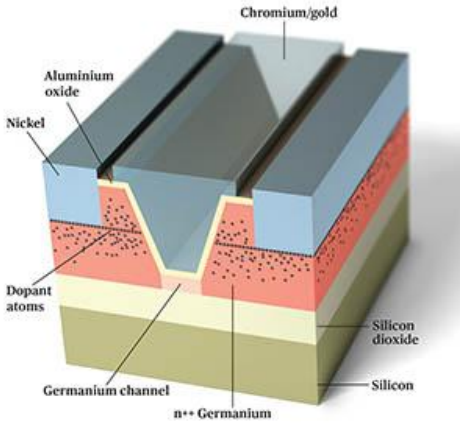

FIGURE 9: Germanium based FET [4].

3. Gallium Arsenide (GaAs) & Indium Gallium Arsenide (InGaAs*):* Combining two elements of group III and group V of periodic tables which has three and five valence electrons, forms a nice substitute for replicating the semiconducting properties in group IV elements. GaAs and InGaAs are two such compounds which show properties of a semiconductor and therefore can be used in

manufacturing FETs. The electron mobility is one such property which receives a huge boost when such compounds are utilized. But due to certain deficiencies in other categories, these compounds are not so ample in the FETs world.

4. Graphene based FETs: Graphene was discovered while analyzing the good optical and mechanical properties. The allotropes of Graphene and Carbon such as fullerenes, carbon nanotubes are certain examples of Graphene based FETs. Graphene also has good electrical properties, and their FETs are used in planar processing technologies. Certain Gate structures in which Graphene channel FETs are back gate, dual gate, and top gate show that Graphene is mainly used in planar transistors. In 2011 IBM designed ICs made of Graphene using the top gate fabrication method. More research and funds have been dedicated into Graphene based FETs by U.S. Defense Advanced Research Projects Agency (DARPA) for communication of airborne military pilots. Graphene based FETs are famous for its RF and Ultra high frequency parameters.

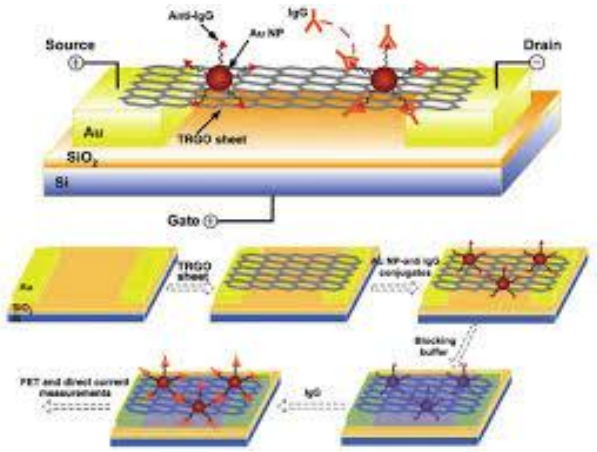

FIGURE 10: Graphene based FET [14].

5. Sensor based FETs: These FETs are application specific due to its characteristic properties acting as a sensor. Certain examples of these FETs are Organic FETs (OFET), GasFET, BioFET, DNAFET, and SiC-FET.

a) OFET: Organic semiconductors are the core component in the electronic material of the FET. These FETs act as sensors for Bio-systems. The main functions of these FETs are to identify the potential of biological systems such as DNA strains, antibodies, and enzymes. Certain OFETs are also used in printing features on plastic. As an example, HP uses these OFETs as a primary component in ink jet FETs. Materials used in Organic FETs are π- conjugated semiconductors in combination with polymers such as poly 3-hexylthiophene (P3HT) and alkyl-substitutes Triphenylamine polymers (PTAA). These OFET devices have good mobility, they are inexpensive, and are made up of biodegradable materials thus giving good sensing capabilities in low-cost fabrication and not adding up in the ever-increasing E-waste production.

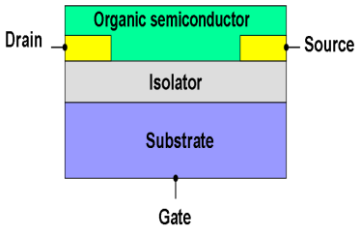

FIGURE 11: OFET Schematic [13].

b) SiC-FET*:* The main environmental concern which has been menacing in the last few years is the air pollution from different greenhouse gases such as SO_2, CO, and NH_3. SiC-FET is the revolutionary FET which is used to sense these SO_2 particles and use it in power generation applications. SiC MOSFETs have very low on-state resistance and high temperature handling capacity. Helping it to find application in power electronic devices such as UPS, DC-DC converters, and fast chargers. STPOWER is one of the companies reaping the benefits of SiC FETs.

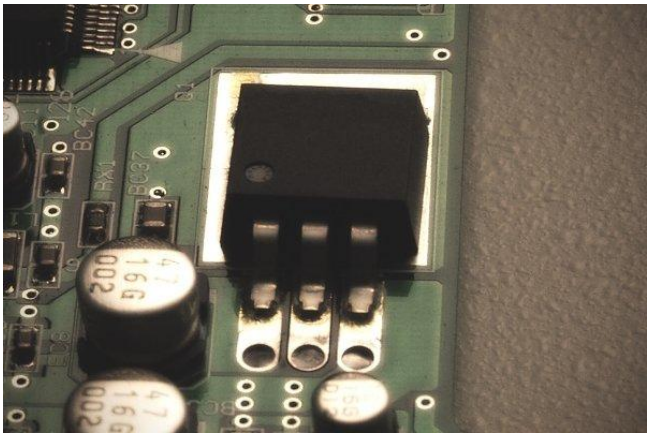

FIGURE 12: SiC Power MOSFET [12].

c) Graphene based GasFET: These sensor-based FETs are sensitive to various gases such as Ammonia, Nitrous Oxide, and water vapor. The semiconductor properties and large surface to volume ratio is pivotal in sensing the various gases. These sensor-based FETs find applications in industries where the above gases are released and help in measuring the quantity of the gas. Thus, it helps in keeping the air pollution in check and maintains sustainability.

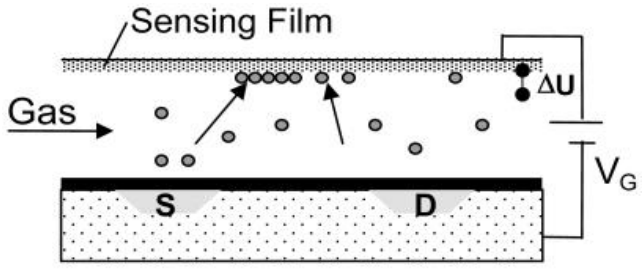

FIGURE 13: Gas FET demonstration [11].

3. COMPARISON BENCHMARKS OF FET

1. Availability of material: As discussed in the above section, FETs are generally made up of semiconductor materials. The most common FETs are made up of Silicon, Germanium, Gallium Arsenide, Indium Gallium Arsenide, Silicon Carbide, Silicon Nitride, Graphene, etc. The most developed and abundantly used materials is Silicon. Since Silicon is easily found in sand, making a transistor out of Silicon is cheap and raw materials are easily available. High investment has been made in manufacturing Silicon based FETs and shifting to a different material would be a huge investment of several billions of dollars. Therefore, it can be predicted that whatever may be the technology or properties of FET, Silicon will be used in majority the FET applications. More than 92% of the FETs are made up of Silicon, closely followed by Germanium and Gallium Arsenide. III-V compounds semiconductors are also used for certain specialized transistors.

2. Switching speed: The rate at which the output of a logic device responds to the corresponding change in input is switching speed. In simple terms, this is the minimum amount of delay to

perform any operation. Switching speed needs to be quick in large power electronic devices such as trains, locomotives, and industrial electronics. Gallium Nitride and Silicon Carbide are the materials which give far superior switching speed characteristics as compared to Silicon and Germanium counterparts. Under similar conditions, Gallium Nitride characteristics show that it outperforms Silicon Carbide. Therefore, to get the best switching characteristics in a FET, non-planar GaN FETs should be considered.

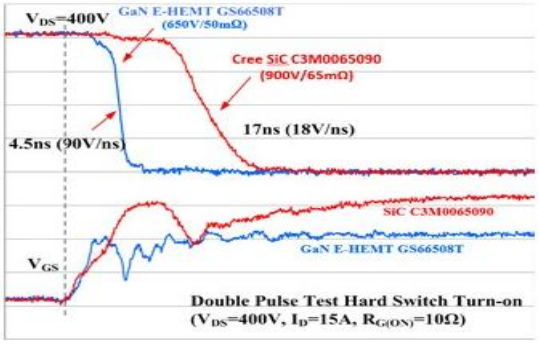

FIGURE 14: Turn-on switching characteristics [6].

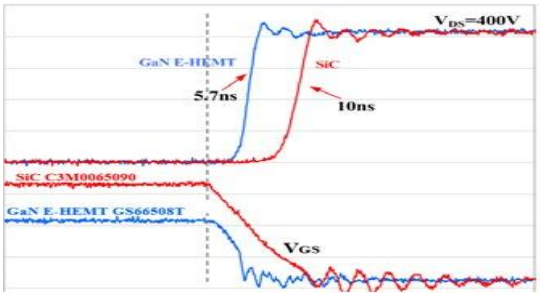

FIGURE 15: Turn-off switching characteristics [6].

3. Ease of manufacturing: Most FETs are manufactured for a certain purpose and application. A proper blend of all the factors must be taken into consideration before deciding which type of FET must be manufactured. Factors include size, dielectric, lithographic techniques, and laboratory setup. Non-planar transistors are the new generation transistors which are used to increase the number of devices on a single chip to help in continuing the Moore's law and provide high performance with high dielectrics. 3D FinFETs are the best FET technology for high density and performance. Though 3D FETs are superior in design, they have multiple manufacturing challenges. The lithography and Ion Implantation on a 3D FET for sizes under 10nm is practically impossible. Most of the FinFETs are manufactured at 28nm. Planar technologies have been used for a while and manufacturers are set up in such a manner that already aid in the production of these planar FETS. Lithography and Ion Implantation technologies are at level 5nm planar structured FETs and are manufactured without tweaking much with the industrial setup.

4. Power dissipation*:* Power dissipation is the amount of power in the form of heat emitted from a FET to carry out a certain task. Less power dissipation results in less leakage and as a result an efficient and a low temperatures device. High temperatures can result in fault and can cause accidental fires which can destroy the hardware. To counter the excess heat dissipation, cooling fans and heat sinks must be employed which increase unnecessary hardware in the system and can cause complexity while designing micro-electronic devices where space is at a premium. To reduce the power dissipation in FETs, minimum voltage drop should be present (V_{DS}). Making

transistor work in a linear mode can help in giving the best performance with minimum power dissipation. FinFETs are the most power efficient devices for the following reasons:

- It has high output current as compared to input voltage.
- Good switching speed and good channel quantization effects better power characteristics. Since the thickness of the FinFET is uniform, there is low variation in threshold voltage. Thus, FinFETs give maximum current with minimum voltage and have low voltage drop making it ideal for applications where minimum power dissipation is needed.

5. Complexity: Complexity is a very important factor as the amount of time and resources spent should be minimum and sustain the high demands of FET hardware required in different junctures of VLSI electronics. The easier the manufacturing process, the less complex is the device and the faster it can be marketed for production. In case some batches are not up to the mark, it will be easy to rectify the less complex hardware design. Since Silicon being abundant and cheap and supporting most of the general characteristics required in a FET hardware, it will have minimum complexity. The compounds such as InGaAs, GaAs, GaN, SiC, and SiN are a fusion of number of elements and hence manufacturing will be complex. Non-planar FETs require certain amount of thickness, a lot of Ion Implantation, complex etching and sharp metal edges making it a complicated manufacturing process. Planar transistors are easy to construct but it has a limitation that it needs to be built in high temperature ovens.

6. Scaling Factors: Scaling is the reduction of length, width, and height of the transistor so that a device can be made small and efficient. Compressing any types of electronic hardware is extremely important as any electronic device needs different hardware for various functions. Providing various parameters such as voltage or lines and channels for transfer of data is extremely tough and if not done properly, there will be a bottleneck and the device will come to a standstill. Scaling in FETs will lead to increase in the electric field in the channel forming Short Channel Effects (SCE). SCE results in issues such as Drain Induced Barrier Lowering (DIBL), Surface Scattering (SS), Hot Electron Effect (HEE), Impact Ionization (II), and Velocity Saturation (VS). When we reduce (scale) the FET, most of the factors are uniformly reduced. But there are certain factors such as V-I characteristics which are not directly scalable, and these factors can affect the power consumption of a device. Scaling in planar type FETs is easier as compared to its non-planar compatriots. As soon as scaling is carried out in planar, the characteristics of the FET are affected. In non-planar devices, these affects are much more and thus scaling needs to be done meticulously.

Large VLSI companies have worked and made sure that the size of the FET can be reduced over time. The technology nodes over the years:

2D technology since 1970 are 10μm -> 8μm -> 6μm -> 4μm -> 3μm -> 2μm -> 1.2μm -> 0.8μm -> 0.5μm -> 0.35μm -> 0.25μm -> 180nm -> 130nm -> 90nm -> 65nm -> 45nm -> 32nm -> 28nm -> and went up to 5nm.

3D technology) -> 22nm (2011) -> 15nm (2013) -> 10nm (2015) -> 7nm (2017) etc., Scaling below 22nm is highly challenging.

7. Thickness: High tunneling current is significant when the thickness (t_{ox}) is less than 1nm. High-k dielectrics such as Zirconia, Hafnium dioxide (HfO_2), are replacement to SiO_2 with acceptable thickness to maintain gate leakage currents within tolerable limits. The t_{ox} cannot be less than 1nm due to high tunneling current and significant statistical variation.

8. Band gap: Silicon has wider band compared to its IV group element Germanium, due to which the leakage of current is less when it is off (Draining power). Also, Silicon has better thermal conductivity which results in less overheat of circuits.

9. Threshold voltage: It is the minimum voltage applied across the gate and source (V_{GS}) which allows the current flow through the transistor. For a given technology node, the threshold voltage depends on oxide and thickness of oxide. Also, body effect influences threshold voltage which is a change in threshold voltage approximately equal to the change in source-bulk voltage (V_{SB}). It acts as a second gate and called back-gate effect.

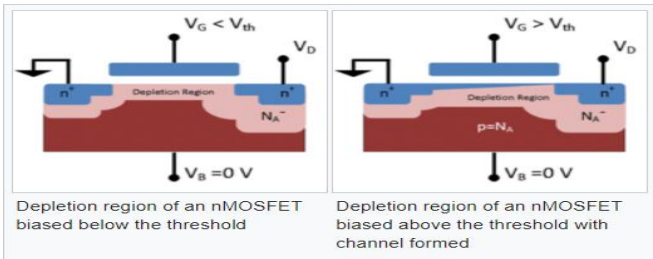

FIGURE 16: Threshold Voltage based on Gate voltage[6].

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

V_{TN} is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, $2\phi_F$ is the surface potential, V_{TO} is threshold voltage for zero substrate bias.

$$\gamma = (t_{ox}/\epsilon_{ox})\sqrt{2q\epsilon_{Si}N_A}$$

γ is the body effect parameter, t_{ox} is oxide thickness, ϵ_{ox} is oxide permittivity, ϵ_{Si} is the permittivity of silicon, N_A is a doping concentration, q is elementary charge.

10. Mobility of charge carriers: Electrons move three times faster than Germanium at room temperature. Holes (the electron voids) are positive charges which move four times faster than Silicon. Less voltage is required for these charge carriers to flow which consume less energy for circuits. Materials like indium arsenide and gallium arsenide also exhibits excellent electron mobility. InAs is 30 times as mobile as silicon. This property does not hold for holes which are not more mobile than Silicon.

Property	Silicon (Si)	Germanium (Ge)	Gallium arsenide (GaAs)	Indium arsenide (InAs)	Unit
Bandgap	1.12	0.66	1.42	0.35	eV
Electron mobility at 300 kelvins	1,350	3,900	8,500	40,000	$cm^2/(V{\cdot}s)$
Hole mobility at 300 K	450	1,900	400	500	$cm^2/(V{\cdot}s)$
Maximum possible electron velocity	1	0.6	2	3.5	$x10^7$ cm/s
Critical electric field	0.25	0.1	0.004	0.002	$x10^6$ V/cm
Thermal conductivity	1.5	0.58	0.5	0.27	W/(cm·K)

FIGURE 17: Materials and their Properties [4].

4. CHALLENGES OF DIMENSION REDUCTION

Impacts Lithography is limited by wavelength of light source. Lithographic techniques like optical lithography, scanning electron beam, and x-ray lithography all have technical problems which require complicated and sophisticated equipment that result in increased manufacturing cost and complexity. It is seen as a cost-effective way by most major manufacturers to maintain the progress than to invest with completely new technology.

5. CHALLENGES OF CHANNEL SCALING

Scaling in FETs will lead to increase in the electric field in the channel forming Short Channel Effects (SCE). SCE results in issues such as Drain Induced Barrier Lowering (DIBL), Surface Scattering, Hot Electron Effect, Impact Ionization, and Velocity Saturation.

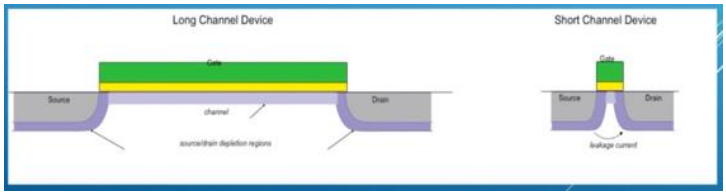

FIGURE 18: Long and short channel transistors [14].

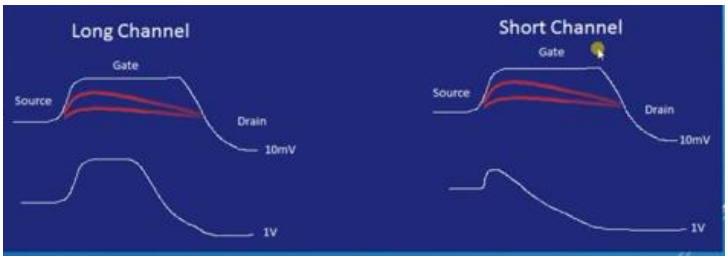

FIGURE 19: Drain Induced Barrier Lowering (DIBL) [14].

1. Drain Induced Barrier Lowering (DIBL): Increase in drain voltage reduces barrier face for electrons and holes and allowing them to pass from source to drain where gate voltage remains unchanged. The slope is called sub- threshold slope in graph II, as the drain voltage increases, the sub threshold slope increases, and the threshold voltage is shifted more which is an unwanted phenomenon.

2. Surface Scattering: E_x is the field due to Vgs and E_y is the field due to Vds. In long channel Ex>>Ey, but in short channel Ex is not negligible. E_x and E_y make electrons to travel on a zig-zag path, reducing mobility. As channel length reduces, E_y increases causing surface mobility to become field dependent.

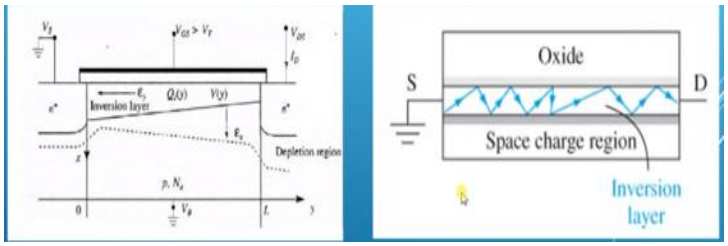

FIGURE 20: Surface Scattering [14].

3. Hot Electron Effect: The energy gained carrier is called hot carrier. Through the zigzag, it gains a lot of energy and crosses the field oxide or gate oxide and goes to the gate. To reduce hot electron, drain is lightly doped, resulting in less electric field for carriers.

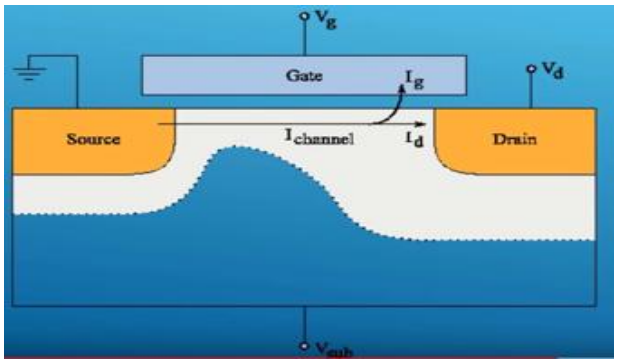

FIGURE 21: Hot Electron Effect [14].

4. Impact Ionization: Electron travelling to drain creates electron-hole pair by Impact Ionization. Secondary electrons are collected at drain, causing current to increase in saturation. Secondary holes are collected at substrate causing to increase latch up.

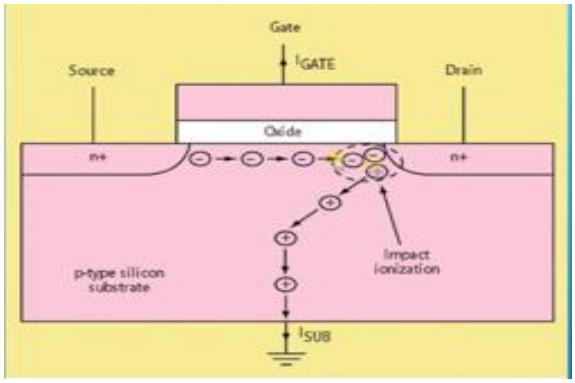

FIGURE 22: Impact Ionization [14].

5. Velocity Saturation: Velocity is proportional to the electric field. After a certain point, velocity saturates and has no effect on the increase in electric field.

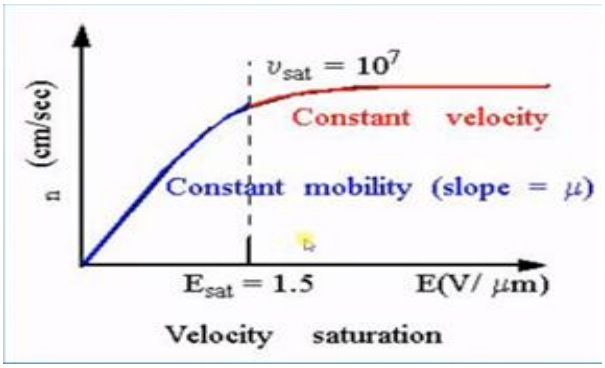

FIGURE 23: Velocity Saturation [14].

6. GRAPHICAL ANALYSIS

Graphical analysis of different parameters helps us in comparing and analyzing the various parameters which affect in the procedure to determine which type of FET is suited along with its parametric comparison.

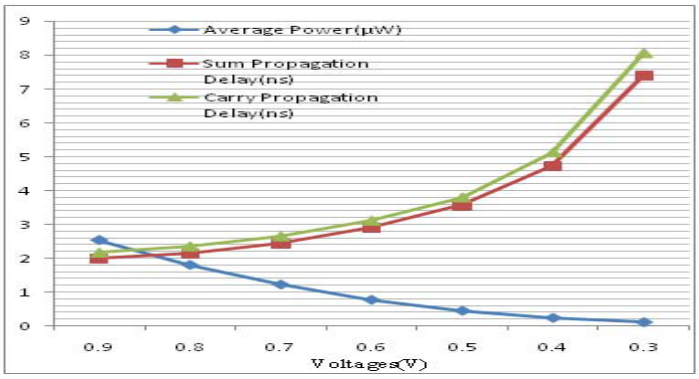

FIGURE 24: Variation of power and delay with input voltage (single-gate) [2].

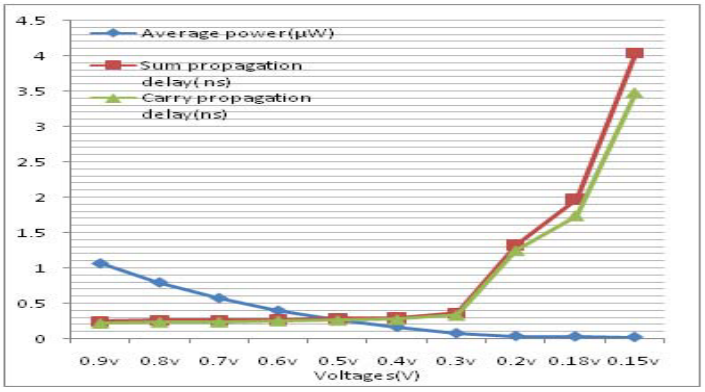

FIGURE 25: Variation of power and delay with input voltage (DGFET) [2].

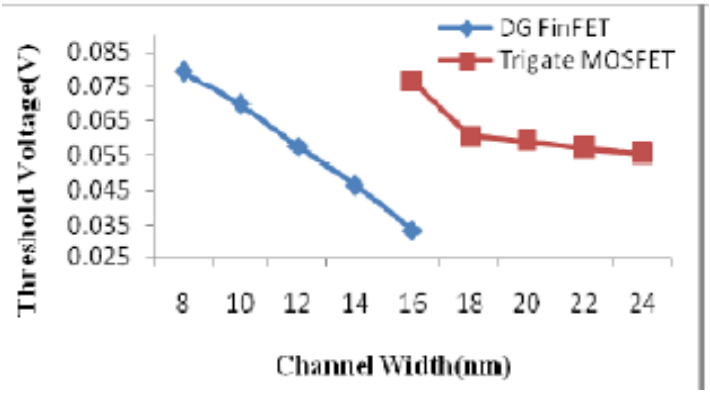

FIGURE 26: Graph for VT sensitivity to channel width variation [1].

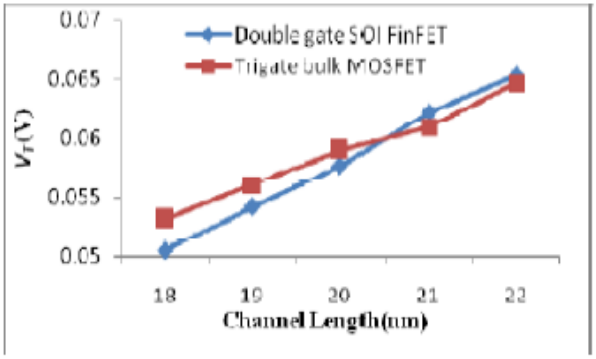

FIGURE 27: Graph for VT sensitivity to channel length [1].

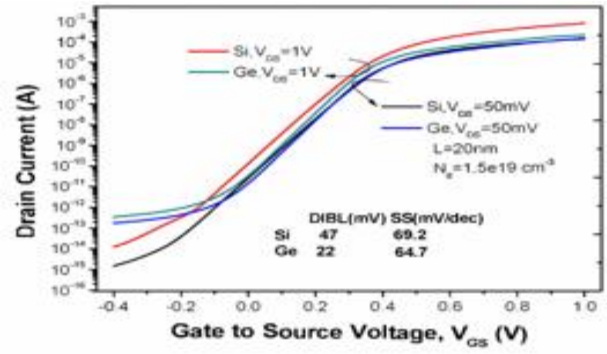

FIGURE 28: Id-V. Characteristics of Si and Ge [8].

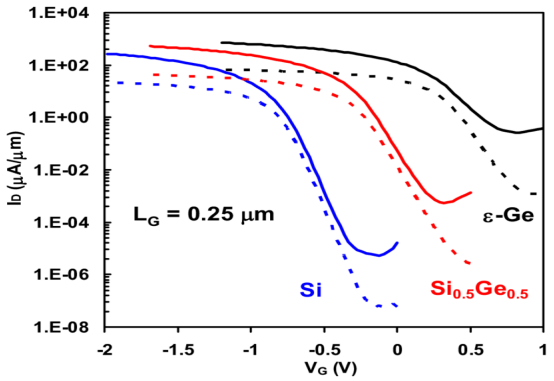

FIGURE 29: Drain current I D vs. gate voltage VG for Si, Si 0.5 Ge 0.5 , and pure Ge channel p-FETs with LG = 0.25 μm showing the exponential increase. [13].

7. IMPROVEMENTS IN PERFORMANCE

Performance in FETs can be improved by using the following technologies:

1. Silicon on Insulator (SOI): The SOI design does further thinning of the body, to achieve fully depleted regime. The Ultra-Thin Body (UTB) Silicon on Insulator (SOI) MOSFET could reduce sub threshold swing near ideal value (60mV/decade). This has heat dissipation issue which cannot be absorbed by the substrate and may affect the operating temperature of the device.

2. Strained SI layer: Increased mobility. By growing epitaxial Si layer on $Si_{1-x}Ge_x$ enhances mobility and reduces scattering. These techniques used by AMD and by Intel (Mistry et al.) many years ago.

3. High-k dielectrics: Materials like Zirconia and Hafnium dioxide (HfO_2) are used as replacement to Sio_2 to maintain acceptable dielectric thickness and to keep gate leakage currents within tolerable limits. Hafnium dioxide (HfO_2) has excellent thermodynamic stability on Silicon, but the soft optical phonons associated with the polarizable hafnium oxygen bonds induced significant reduction of the electron mobility and reduced transistor performance. Researchers substituted polysilicon gate electrodes with metal gates to recover a portion of the channel mobility.

8. ANALYSIS BASED ON STATS

The above discussed benchmarks provide a good guide to be able to compare which technology FET should be considered in the design and implementation of a product.

For microelectronics such as small memory elements, ICs, and logic switches, commonly used FETs which form a good fit, are the trivial ones made by Silicon. Simple arrangements are required for minimum power dissipation. Smaller planar FETs made up of silicon form a good fit as the hardware can be readily available and cheap. Designing these FETs should not be complicated and can be easily produced in large quantities as small microelectronics should be manufactured using simple planar FETs, made up of silicon.

For embedded system microcontrollers and microprocessors, power dissipation, space in the chip, memory of the chip and the switching characteristics with high mobility is required. In these types of electronic products, budget may be a concern but rather than a certain application, these are general purpose electronic systems which find their application in various fields. They are mainly real time operating systems where a fast output is required. At this juncture, FinFETs and Gate all around (GAA) FETs are extremely useful. Materials such as Carbon-Nano-Tubes (CNTs) and Germanium nanowires and these FETs require less space, and many numbers of ICs are embedded in a single wafer. It gives high performance and can be utilized as a hardware component of embedded system. Embedded Systems and their chips are used in mobile phones, smaller computers, washing machines, air conditioners, television sets, etc.

For electronics used in the communication field such as radio frequency devices, devices must be small, should be able to work in ultra-high frequency range and should be able to communicate. These devices are made for encoded communication for defense purposes and satellite communication. Graphene based FETs are extremely useful for these types of electronics as they help in transmitting and receiving data wirelessly. For this reason, planar FETs made up of Graphene can be useful for communication electronics such as Bluetooth and Wi-Fi modules.

For large industrial electronics switching speed needs to be fast. Devices need not be compact and power dissipation may be high. For high investments, a single device with utmost precision must be manufactured. During such applications, FETs must be non-planar FinFETS with channel material constituting of Gallium Nitride and Silicon Carbide which can provide high power dissipation, high efficiency and high switching speed.

9. RESULTS

Our main aim was to categorize FETs which can help as a foundation for artificial intelligence. Embedded systems are programmed and trained with machine learning and deep learning algorithms by devising training sets and neural networks. Analysis of these devices must be accurate and high memory cells should be present so that abnormalities can easily be categorized to make sure that the devices are error free. After analyzing all the benchmarks and categorizing the FETs, we propose that 3D non-planar FinFETs made up of silicon or germanium is very useful. Along with these FinFETS, the embedded systems can use sensor based Organic

FETs that are very useful as training algorithms can stored in FinFETs and can be quickly matched and analyzed by these sensors. Organic FETs are biodegradable, which make them extremely useful, and they help in reducing the pollution. Chip manufacturers and semiconductor companies such as Intel Corporation, Texas Instruments, Advanced Micro Devices and NXP Semiconductors are using non-planar FETs as the foundation for the hardware.

10. CONCLUSION AND FUTURE WORK

We believe a strong, accurate, and efficient hardware can be the ideal foundation for the next generation electronic devices and algorithms for accurate and expeditious output. FET is the basic and a very important hardware for all embedded system electronics and Internet-of-Things (IoT) components. By understanding and analyzing the hardware of the FET technologies, we were able to categorize various FETs technologies and recommended the better performed technologies to help designers and the users to understand and efficiently use the hardware required for their applications. This paper helps interested researchers in the field in understanding and advancing the-state-of-the-art FET technology to the next level and in moving to newer generation FET technologies and in setting up even better-quality hardware which can meet the high level of performance the global electric/electronic and computer science communities' demand.

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