A Novel Topology Of Delta Modulation Technique For Improving The Power Factor Of Ac-Dc Converters

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Abstract

This work presents a new topology of delta modulation technique. This kind of modulation technique is usually used to improve the power factor of Pulse Width Modulation (PWM) converters used for supplying A.C. drives. Many new topologies have been presented trying to obtain a cost-effective solution to reduce the input current harmonic content and to make it sinusoidal and in phase with the input voltage of AC-DC converters. Each one of them has its application range due to the inherent characteristics of the topology (See [2-3]).

Obviously, not every converter is useful for the same application. Hence, this paper tries to show the most appropriate topology of different variants of modulation technique used for power factor correction. This technique which is used to generate the PWM control signals for the main devices of the PWM converter has the advantage of yielding instantaneous current control, resulting in a fast response [3], [4]. However, the switching frequency is not constant and varies over a wide range during each half-cycle of the A.C. input voltage. Furthermore, the frequency is also sensitive to the values of the circuit components, which is also addressed in this paper. This new delta modulation technique topology proves to give great stability performance over other variants of delta modulation or other modulation techniques.

Keywords: AC-DC Converter, Delta Modulation Technique (DMT), New Topology, Power Factor (PF), Simulation and Modulation.

1. INTRODUCTION

It is well known that the input voltage and current waveforms of ideal AC-DC converters are sinusoidal and in phase. However, the current waveforms of practical AC-DC converters are non-sinusoidal and contain certain harmonics. As a result of that, the phase shift between the input current fundamental component and the voltage of AC-DC converter is increased. The power factor (**PF**) which depends on the delay angle of AC-DC converter, the phase shift between the input current and voltage and the circuit component are then reduced [8]. With the aid of modern control technique and the availability of high speed semiconductor devices, the input current can be made sinusoidal and in phase with the input voltage, thereby having an input power factor of approximate unity.

Delta modulation, also known as ripple controller control, maintains the AC-DC converter input current within a defined window above and below a reference sine wave. The greatest benefits of delta control are that it offers fast load transient response and eliminates the need for feedback-loop compensation. The other well-known characteristic is the varying operating frequency.

However, the regulation inaccuracy issue of the delta controlled converter is almost unknown to engineers. Until now, research on delta controllers has mainly focused on transient analysis and transient modeling [1-3]. The first analysis of accuracy was performed on a current mode delta controller specifically designed to power microprocessors [5]. However, the regulation accuracy of the more widely used current-mode delta-controlled controllers is still unknown.

Furthermore, bang-bang technique used in [2] for the same purpose as DMT suffers from certain drawbacks. For example, it does not enable a simple realization of the shifted switching of the bridge converters that are connected in parallel. The shifted switching evidently reduces the ripple of the current derived from the trolley. It also requires a very fast microprocessor since it needs a very short current sampling period.

In this paper a new topology with new algorithms for generating the PWM control signals for the transistors of the converter is introduced to delta modulation technique (DMT). These new algorithms are solved by using high frequency semiconductor devices and suitable control circuitries. The result of using such algorithms is not only improved performance of the converter, and optimal waveform of the current derived from the trolley, but also the shifted switching of the parallel connected converters will be no longer needed [3], [7].

The remainder of the paper is organized as follows: Section II presents the principle of operation and an overview of the algorithms used for switching the transistors of the converter. Different logic algorithms and some simulation obtained as a result of using these algorithms for delta modulation is shown in Section III. Finally, Section IV gives the conclusions to the paper.

2. PRINCIPLE OF OPERATION OF DMT

Figure 1 shows a unity PF circuit that combines a full bridge AC-DC converter and a full bridge voltage inverter (frequency converter). The control circuits of AC-DC converter have two main functions:

- Ensuring a unity PF (sinusoidal current which is in phase with the input voltage).
- Ensuring a constant voltage U_d across the capacitor

The first function 1 can be easily realized, as the boundary values of the hysteresis band I_{w2} and I_{w1} are generated such that the 1^{st} harmonic component of the current derived from the trolley is in phase with the voltage, as will be shown later in the paper. The switching transistors change their state as soon as current I_{sa} reaches the reference boundary value of the hysteresis band.

The second function is obtained by using a voltage controller R_v of voltage U_d which generates a suitable value for the reference current I_{ref} that is derived from the trolley (during motoring regime $I_{ref}>0$, and during braking regime $I_{ref}<0$). From the simulation obtained in the next sections it is clearly evident that there is a certain relationship between the amplitude of current I_a, current I_d, current I_c and consequently with voltage U_d at the output.

The voltage controller R_v regulates the mean value of voltage U_d which is always estimated at the instant of sampling of R_v. With respect to the required current waveform it is good to have I_w constant during each halve cycle of the required current.

This delta method of control keeps the input current I_{sa} within the window hysteresis band around the reference current I_{ref} which leads the sinusoidal value of this current I_a to be in phase with the sinusoidal voltage U_a and without any dc offset. To obtain a sinusoidal current the sampling of the controller must be synchronized with the current waveform and the sampling period must be $TT = 0.01$. A new value of I_{ref} must be estimated exactly at the zero-crossing of current I_a.

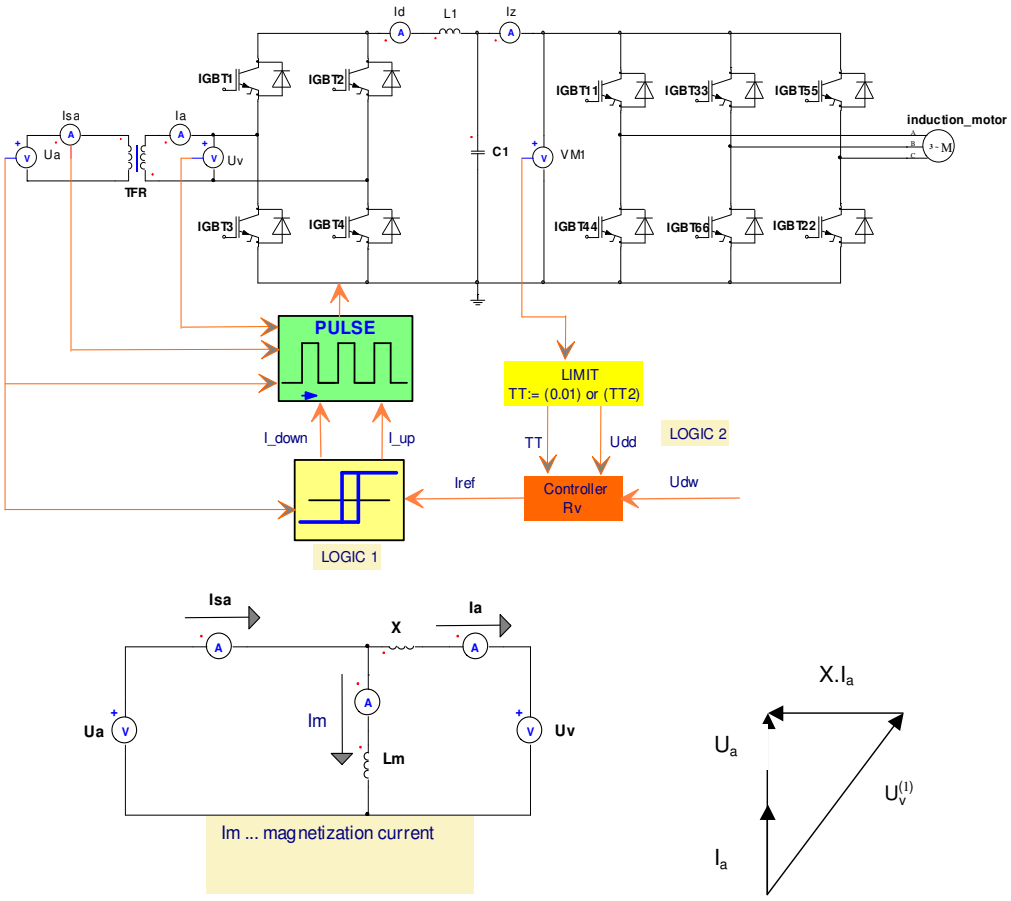


FIGURE 1: FREQUENCY CONVERTER CIRCUIT ARRANGEMENT FOR UNITY PF

This conclusion is based on the assumptions that filter L_1, C_1 at the output of the AC - DC converter is not added into the dc circuit and that all components used are ideal. However, in practical applications, these assumptions have certain types of error. Output voltage ripple also includes output capacitor C_1-caused ripple and L_1-caused ripple. And all components used are not ideal, so there will be delay in the whole control loop. Given these realities, the current waveform I_d then includes a clear harmonic component of frequency $f = 100\,Hz$. This component increases the ripple of current I_d and voltage U_d.

When the controller sampling period is $TT = 0.01s$, then the output of the controller under steady state conditions I_{ref} is purely constant. The sampling period TT of R_v may cause a time delay in the voltage control circuit. Therefore, it is necessary to reduce TT during transients. This therefore will result in a staircase waveform of the current but the dynamic properties of the voltage control loop are improved substantially.

Figure (1) shows clearly how the voltage and current derived from the trolley are measured. It is therefore evident that voltage U_a must be measured at the primary side of the transformer. The current on the other hand, may be measured at the secondary side since current I_a may be obtained as the average value of current I_{sa}.

3. LOGIC 1 USED FOR SWITCHING OF MAIN TRANSISTORS

Figure 2 shows the transistor rectifier circuit with the PWM control signal algorithm of the buck regulator circuit which may be connected at the output of the rectifier. This buck regulator is not considered in this paper. Logic1 demonstrates the algorithms used in delta modulation for generating PWM gating signals for the main transistors of AC-DC converter. The switch state of AC-DC converter is in general determined by comparing U_v with U_0, where U_0 is an arbitrary voltage determined as follows: $0 < U_0 < (U_d)\min$. Around the zero-crossing of voltage U_a, voltages $+U_d$, $-U_d$ are applied alternatively at the ac input terminals of AC-DC converter.

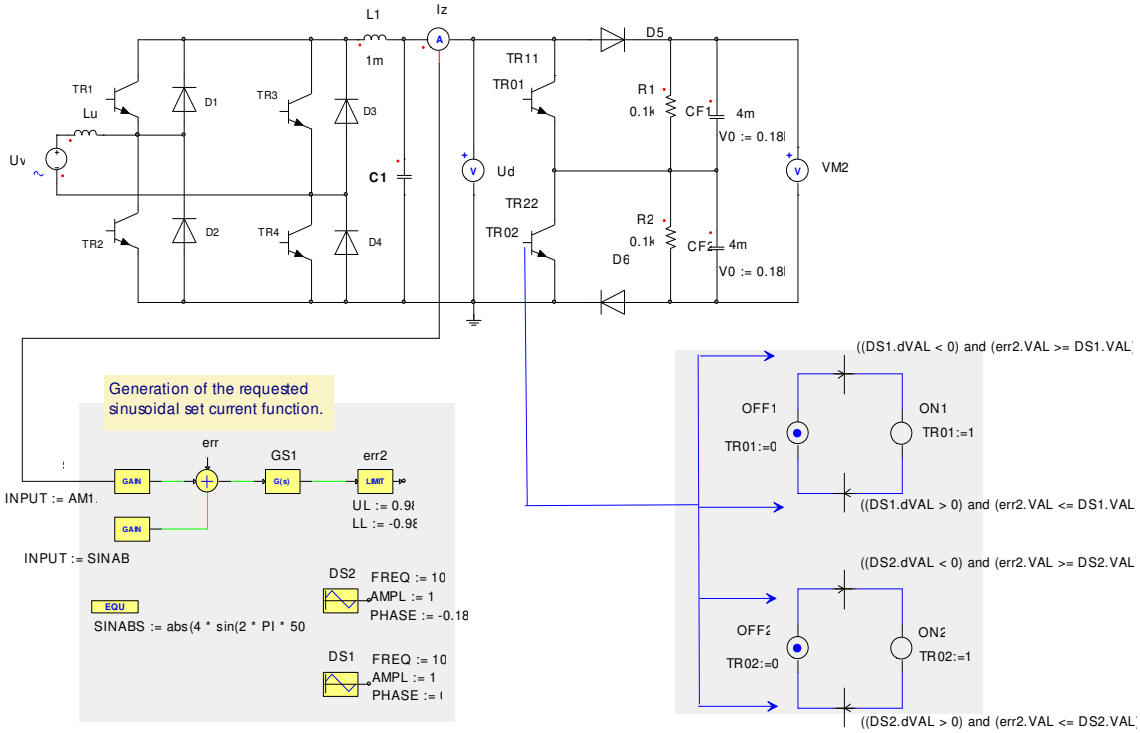


Figure 2: Rectifier circuit with control algorithm of the buck regulator used at the D.C. side of the rectifier

3.1. First variant of Logic 1

The simulation of the rectifier circuit is carried out under the following conditions:

- $I_{sa} < i_{\_down} \ldots U_v = 0$
- $I_{sa} > i_{\_up} \ldots U_v = U_d$
- $i_{\_down} < I_{sa} < i_{\_up}$ … hysteresis effect
- U_0 … arbitrary voltage ($0 < U_0 < U_{d(\min)}$), the switching state of the converter is determined by comparing U_v with U_o.

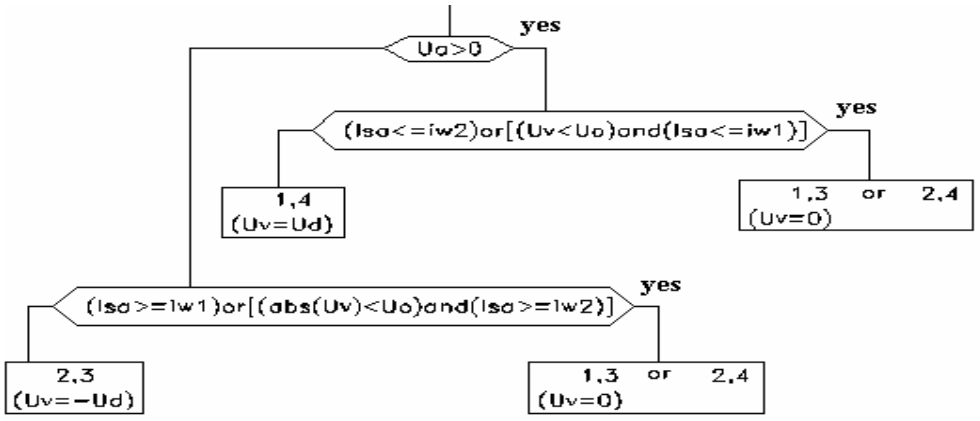
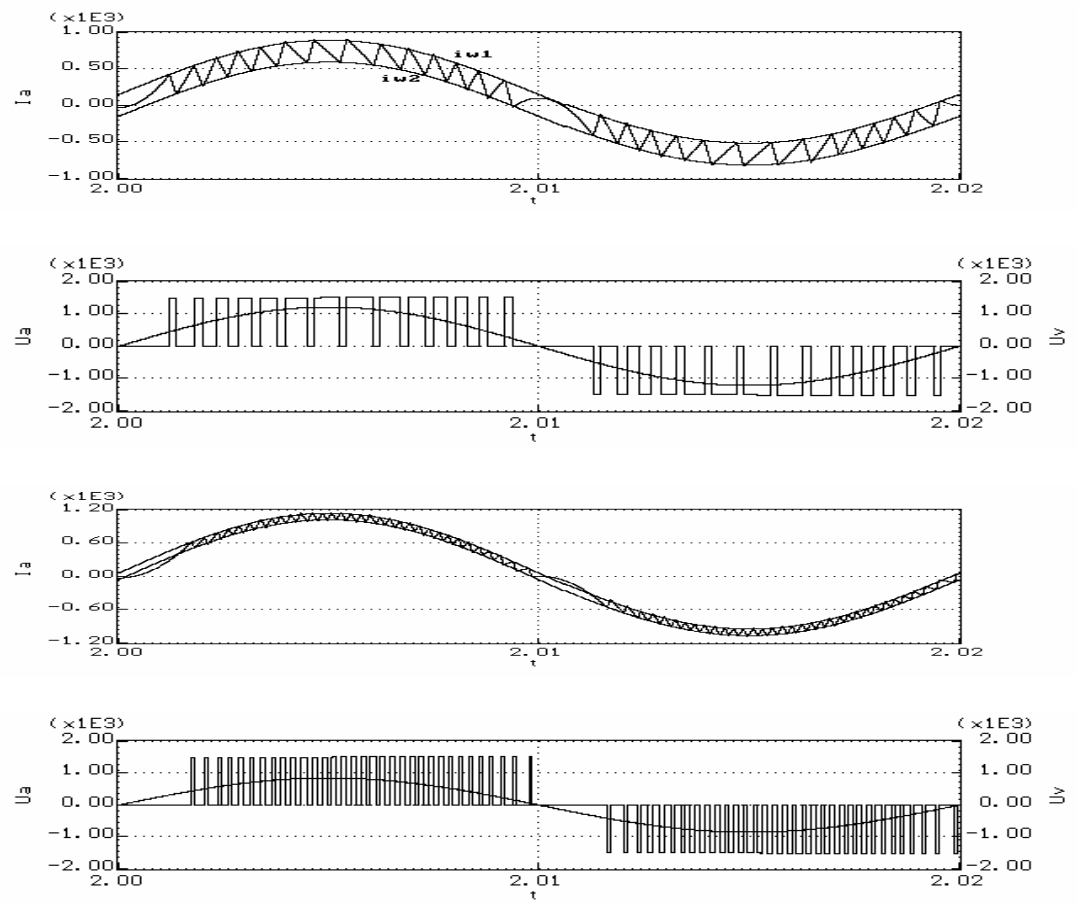


Figure 2a: Variant 1 of Logic 1



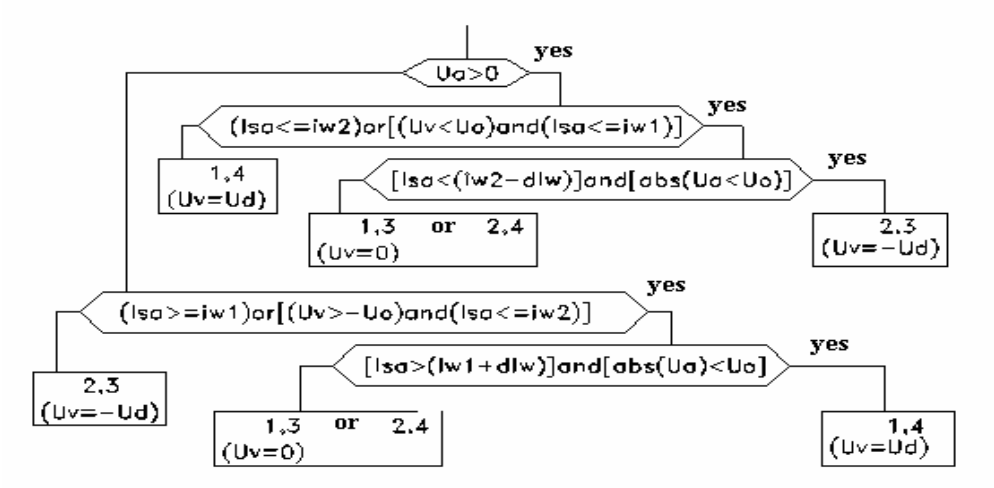
$$\Delta I = 60A\text{, } U_a = 70\%\ of\ U_{an}$$

Figure 2b: Simulation results of variant 1

Note: Concerning this variant of Logic 1, as it is seen of the above simulation, current I_a leaves the window limits around the zero-crossing of U_a which adds a certain drawback to this variant. Current I_a also increases very slowly when U_a is so small.

3.2. Second variant of Logic 1

To force current I_a to stay within the given hysteresis window limits I_{w1}, I_{w2}, then in accordance with the required current, voltage U_d must be applied instead of a zero voltage across the a.c. terminals of the converter. The algorithm with the results obtained is illustrated in figure 3 shown below.



dI_w … tolerance current ripple

U_0 … arbitrary voltage ($0<U_0<(U_d)_{\min}$) (comparing U_v with U_0 determines the switching state of the converter)

Figure 3a: Variant 2 of Logic 1

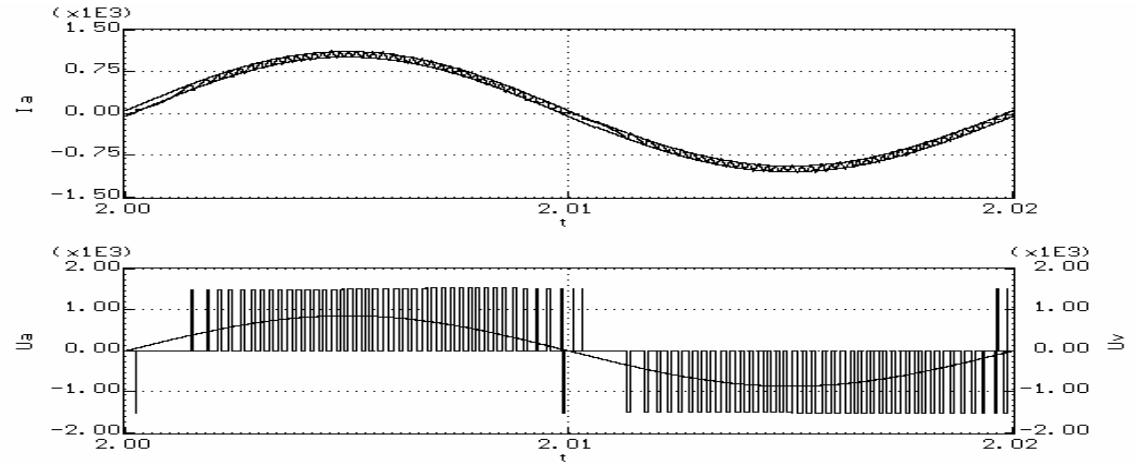
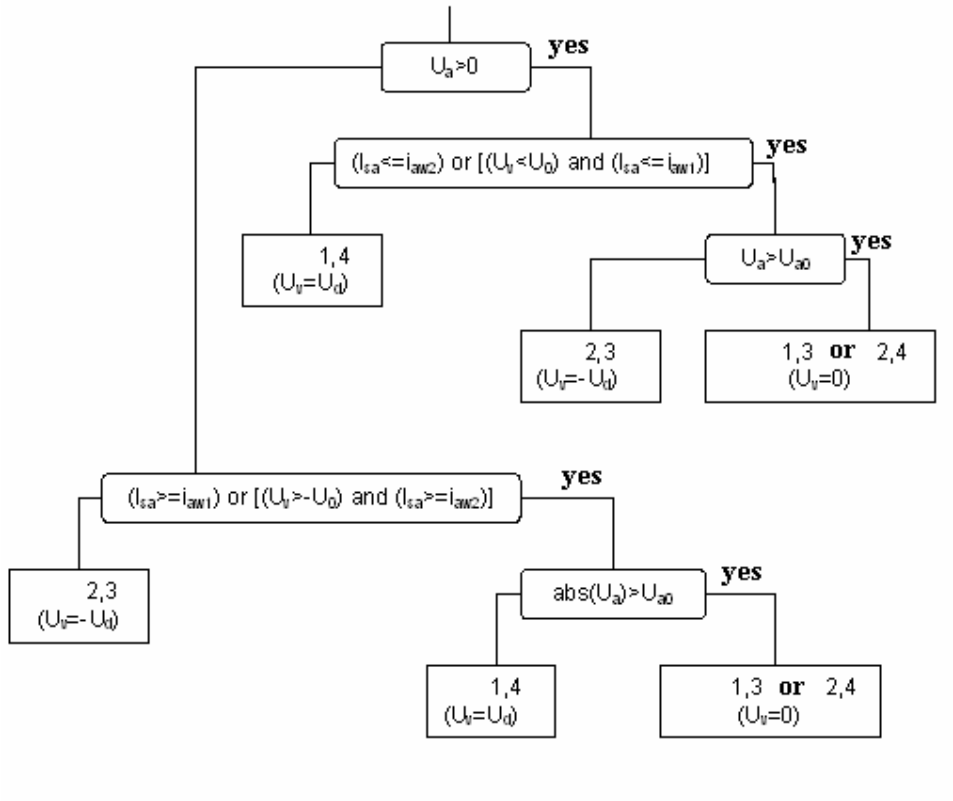


Figure 3b: simulation results of variant 2

3.3. Third variant of Logic 1

To improve the voltage waveform around zero-crossing shown in figure 2b, voltages $+U_d$ and $-U_d$ are applied alternatively at the a.c. terminals of the converters. Variant 3 of Logic 1 and the simulation results of this variant are shown in figure 4.



U_0 … arbitrary voltage, ($0<U_0<(U_d)_{\min}$) and again comparing U_v with U_0 determines the switching state of the converter.

If $U_a<U_{a0}$, then the function of Logic 1 is changed.

Figure 4a: Variant 3 of Logic 1

4. LOGIC 2 FOR DETERMINING THE SAMPLING PERIOD TT OF CONTROLLER RV

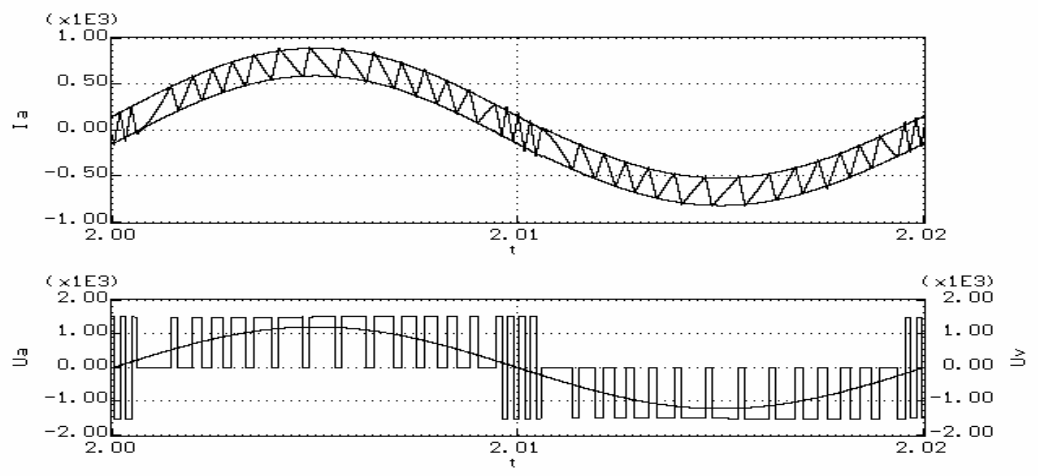
Logic 2 in Figure (5) explains the algorithm used to test the sampling period TT of R_v. The operating period of the voltage controller R_v is divided into samples. If the deviation between the mean value of the voltage across the capacitor U_{dd} during the sampling period TT and the given dc reference is greater than ΔUd, a shorter period TT2 is then applied. In our simulation example we consider the dc reference voltage to be 1500V. Using this technique, the output voltage U_d is always forced to remain within a fixed given value, and this exactly what is needed.

- TT is the sampling period of R_v.
- TU is the sampling period of voltage U_d.
- U_{dd} is the mean value of voltage U_d over period TT

5. VARIANT 3 OF LOGIC 1 - BEST SIMULATION RESULTS

A demonstration of delta modulation using the above mentioned algorithms is prepared using Matlab 6.5 and software programming language "Pascal". Such work was carried out under the condition of negligible magnetization current. This current is shifted by 90° with respect to voltage U_a because of the prevailing leakage flux at the secondary side of the transformer. The current I_a is forced to remain between the upper and the lower limit of reference window band. To achieve this result, the primary

current I_{sa} is compared with I_{w1} and I_{w2}. For the same purpose voltage U_v is compared with an arbitrary voltage U_0 whose value must be greater than zero and smaller than the minimum value of U_d (as depicted in figure 3). The results of using different algorithm variants for implementing delta modulation technique is current I_a and voltage U_a as it is shown in figures 2, 3, 4. The fundamental components are in phase and therefore, by deploying this means of control, the target of improving the power factor of AC-DC converter is achieved. However, variants 3 gives better results than variant 1 and 2 as it is shown in figure 5, 6 and 7.



$$\Delta I = 150\,A, U_{a0} = 200V$$

Figure 4b: Simulation results of variant 3

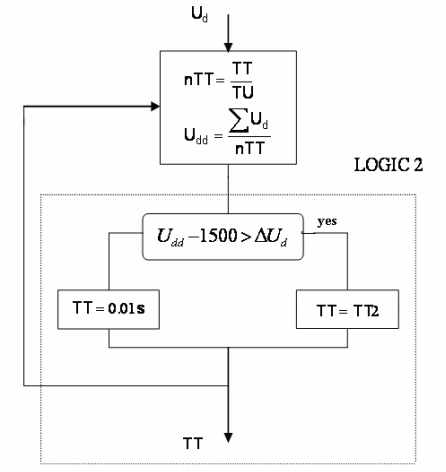


Figure 5: Logic 2 used for testing TT of R_v

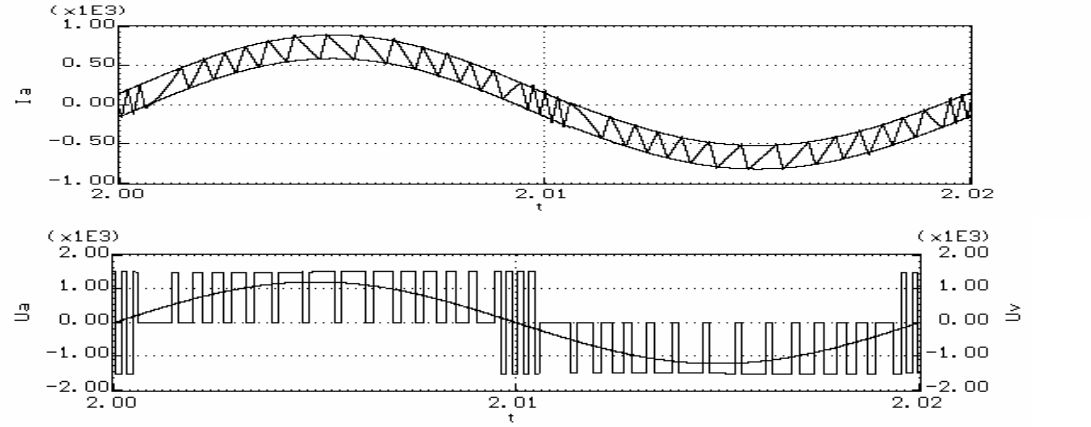
Figures (5, 6 & 7) below are graphical representations of variant 3 - Logic 1 and Logic 2. These figures are obtained under the conditions of disconnected and connected filter at the output. The aim of logic 2 is to obtain a constant voltage at the output of AC-DC converter and the input of the voltage inverter.

6. CONCLUSION

Many new modulation techniques have been developed to improve the performance of the AC-DC converters. It can be concluded that, by controlling the input current of a bridge AC-DC converter with the aid of a suitable control technique, the input current of AC-DC converter can be made sinusoidal and in phase with the input voltage, thereby having an input PF of approximate unity, resulting of a more stable performance of the system. This paper presents a new topology (logic variant) of delta modulation technique used for this purpose. Variant 3 introduced in this paper gives better simulation results compared to variant 1 and variant 2.

The reference dc voltage value for U_{dd} was considered in this paper to be 1500-V. Concerning the filter used at the output of AC-DC converter to filter out the high harmonics generated there it may badly affect the dynamic properties of the motor. The simulation however shows that the parameters considered as optimal for the motor without a filter are suitable even for a motor with a filter.

On the other hand the converter can be combined with a high frequency single phase buck-boost converter to reduce the size of the filter. This combination will allow the use of the filter, reduce its bad effect on the motor and make the power factor at the input of the converter more closed to unity.



ΔI = 150 A, U_{a0} = 200 V

Figure 5: Input voltage and current waveforms

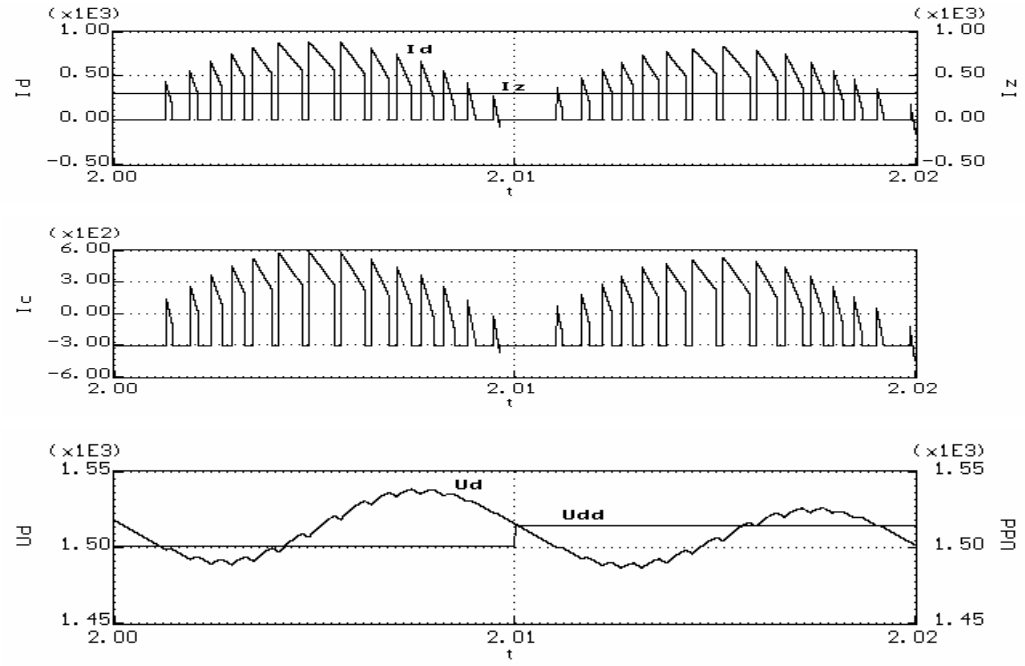


Figure 6: Output voltage waveforms obtained for a disconnected output filter L1, C1.

- $TT = 0.01s, T1 = 1/50000\,s, \Delta I = 150\,A$
- $measuring\ period\ of\ voltage\ U_d\ is TU = 1/1000\,s$
- $Operating\ period\ of\ voltage\ regulator\ R_v\ is\ \mathrm{var}iable$
- $Transformer\ \mathrm{sec}ondary\ voltage\ U_{an} = 860V$
- $No\ \mathrm{min}al\ \mathrm{sec}ondary\ current\ I_{an} = 663\,A$
- $Short-circuit\ volatge\ of\ a\ transformer\ e_k = 30\%$

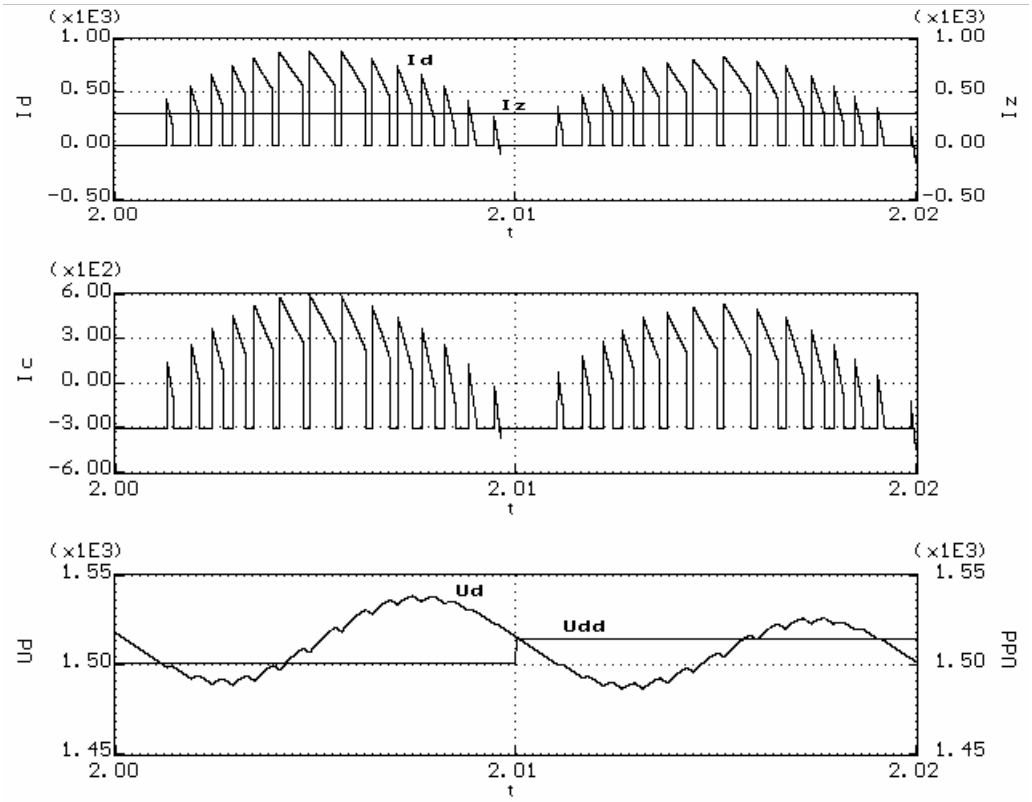


Figure 7: Output voltage waveforms obtained with a connected output filter L_1, C_1, filtr $C_1 = 8\,\text{mF},\ L_1 = 0.316\,\text{mH}$.

- $TT = 0.01s,\ T1 = 1/50000\,s,\ \Delta I = 150\,A$
- *measuring period of voltage* U_d *is* $TU = 1/1000\,s$
- *Operating period of voltage regulator* R_v *is* variable
- *Transformer secondary voltage* $U_{an} = 860V$
- *No minal secondary current* $I_{an} = 663\,A$
- *Short – circuit voltage of a transformer* $e_k = 30\%$

LIST OF ABREVIATIONS	
I_{sa}	Transformer primary current, derived from the trolley at the A.C. side of AC-DC converter.
I_a	Transformer secondary current, at the A.C. side of AC-DC converter
U_a	Primary voltage at the A.C. side of AC-DC converter
U_v	Secondary voltage at the a.c. terminals of AC-DC converter
I_d	Current flowing into the d.c. circuit of AC-DC converter
I_{c1}	Current flowing into filter L_1, C_1
I_z	Current derived by the inverter
U_{dw}	Desired voltage of the capacitor
U_d	Voltage across capacitor C_1
U_{dd}	Average value of the voltage across the capacitor during TT
TU	Sampling period of voltage U_d
TT	Sampling period of voltage controller R_v
T1	Current sampling period
nTT=TT/TU	Number of voltage samples during TT
I_{ref}	Desired amplitude of the current derived from the trolley
$I_{\_down}$, $I_{\_up}$	Window band Limits
ΔI	$I_{\_up} - I_{\_down} = 2.\ \Delta I$

U_0	$0 < U_0 < (U_d)_{min}$. U_0 is an arbitrary voltage used by logic 1 to test the state of the converter
U_{a0}	$U_a < U_{a0}$ … function of logic 2 is then changed
ΔU_d	Voltage deviation on which Logic 2 reacts (from the average value of the voltage across the capacitor)

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