# Extremely Low Power FIR Filter for a Smart Dust Sensor Module

**Md. Moniruzzaman** *monir_706@yahoo.com*
*Department of Electronics & Telecommunication Engineering*
*Southeast University*
*Dhaka, 1207, Bangladesh*

**Md. Murad Kabir Nipun** *nipun83_aiub@yahoo.com*
*Department of Electrical & Electronic Engineering*
*Southeast University*
*Dhaka, 1207, Bangladesh*

**Sajib Roy** *sajib_roy22@yahoo.com*
*Department of Electronics & Telecommunication Engineering*
*University of Liberal Arts Bangladesh*
*Dhaka, 1209, Bangladesh*

**Abstract**

Digital filters are common components in many applications today, also in for sensor systems, such as large-scale distributed smart dust sensors. For these applications the power consumption is very critical, it has to be extremely low. With the transistor technology scaling becoming more and more sensitive to e.g. gate leakage, it has become a necessity to find ways to minimize the flow of leakage in current CMOS logic. This paper studies sub-threshold source coupled logic (STSCL) in a 45-nm process. The STSCL can be used instead of traditional CMOS to meet the low power and energy consumption requirements. The STSCL style is in this paper used to design a digital filter, applicable for the audio interface of a smart dust sensor where the sample frequency will be 44.1 kHz. A finite-length impulse response (FIR) filter is used with transposed direct form structure and for the coefficient multiplication five-bit canonic signed digit [7] based serial/parallel multipliers were used. The power consumption is calculated along with the delay in order to present the power delay product (PDP) such that the performance of the sub-threshold logic can be compared with corresponding CMOS implementation. The simulated results shows a significant reduction in energy consumption (in terms of PDP) with the system running at a supply voltage as low as 0.2 V using STSCL.

**Keywords:** STSCL, CMOS, PDP, CSD Multiplier, FIR Filter.

## 1. INTRODUCTION

This Smart dust is a new and emerging technology in the fields of small wireless sensor development. They are very small and each sensor has the capability of communicating with other sensors. They are run by battery power supply and its lifetime depends on the application and environment it is being used by. Currently these sensors are applied in forest services and in chemical plants. The basic purpose of these sensors are to gather important data (excluding noise or unwanted data) from the environment it is being applied to, and then transfer them to a main server by wireless medium. It has basic DSP (digital signal processing) sections to perform processing of the gathered input signals. One of the key components of that DSP section is a digital filter which is required for eliminating any unwanted signals or noise. It is important for the longevity of these sensors that they should consume as low power/energy during application (without degrading performance by too much) and have a long lasting battery life. For achieving such longevity in respect to battery life, the digital sections of these sensors need to be run under lower supply and also dissipate as low leakage as possible. But it has to be kept in mind system performance or delay must not be harmed by great amount in the course of reducing supply voltage. Thus low power and low energy consumption with desirable performance are highly

demanding requirements in the field of small-scale sensor applications. Integrated circuitry used in these types of sensors must be efficiently employed and optimized such that the overall system consumes very low energy from its battery or source of energy without any or with minor degradation of performance. For current MOSFET processes at channel lengths below 65 nm the leakage currents and its impact on performance has become a factor of concern. At a 45 nm node, or below, the trend is that the leakage current continues to have a negative impact on performance as well as the energy consumption. The usage of dynamic voltage scaling can reduce the dynamic energy dissipation, but quite often this also increase the leakage current. Further on, in 45 nm or lower the gate-to-channel tunneling effects is a large contributor to the overall energy consumption. Leakage current can also consist of subthreshold leakage, which is significant during the off-state operation mode. In CMOS the sub-threshold leakage can be reduced by using MOSFET devices with high threshold value which in turn narrows down the possible range for voltage scaling. Further on, reducing supply voltage in attempt to reduce power consumption has a drawback as it increases the propagation delay. So even though power consumption is less but due to larger delay - the energy consumption of the system increases, hence performance as well as battery life for the system degrades. The mentioned drawbacks can be solved using several different techniques like power gating [1] or multi-threshold CMOS libraries [2]. In some sense, this increases the design complexity and imposes difficulties for the verification and verification tools. For example, we might have to introduce several different clock domains and power modes/domains to maintain the system performance under all conditions. Thus the use of new types of logic styles, instead of CMOS, is a welcomed approach. Sub-threshold source coupled logic (STSCL) is a fairly new kind of logic style that have recently came into consideration for its ability to operate and perform at sub- threshold region ($V_{in} < V_t$) of a MOSFET device [3]. This operating ability at sub-threshold or linear region allows the use of gates implemented with STSCL and they can be operated at very low supply voltage without little harm on system performance. Thus providing a low energy consumption rate for a system implemented with STSCL gates. The understandings of the STSCL topology is applied to a fifth-order FIR transposed direct form filter. We are aware that FIR filters might require more computational power, but as we are focusing on observing the advantages of using STSCL topology over CMOS in terms of energy consumption, this type of filter architecture is better suited for serving the purpose. The basic STSCL inverter circuit and the required bias circuit for operating the logic at sub-threshold region have already been designed and tested in other research papers [1]. Thereby focus in this specific paper is given on the STSCL implemented gates needed for filter designing, and the minimal configuration at which the gates can operate suitably. Section II and III insights on the implementation of the STSCL based gates, the amplifier needed for the replica bias circuit and the 5th order filter in STSCL gates. Finally the paper concludes with the comparison of their performance with CMOS gate implementation.

## 2. BASIC LOGIC GATES IN STSCL

The Exclusive or (XOR/XNOR), or (OR/NOR), and (AND/NAND) gates, along with flip-flops (DFF/DNFF) are the most commonly required logic gates to design a digital filter that will be applicable to smart dust sensor modules implementation. The logic gates are designed to perform under sub-threshold region at scaled down supply voltages; down to 0.2 V. The provided bias currents per stage are in the order of 250 pA. The PMOS (acting as high resistive load [4]) widths are 135 nm (has to be low in order to achieve a high load resistive value, this is mandatory for running the gates at sub-threshold region) and the NMOS input devices are off widths 675 as they need to have stronger driving capability to perform full logic swing of the next logic stages.. The circuit schematics for the XOR, OR, AND gates and DFF are given in Figure 1. The results of performed simulations on XOR, OR and AND given in TABLE 1. The simulations are performed with inputs at a rate of 10 kHz. For the DFF a clock frequency of 44.1 kHz is applied with the input data rate at 10 kHz, like before, and an output duty factor of 50 %.

| Logic | Temperature | Power[nW] | Delay [µs] |
|---|---|---|---|
| XOR/XNOR | - 20 | 0.152 | 2.52 |
| | 70 | 1.11 | 0.096 |
| OR/NOR | -20 | 0.157 | 1.489 |
| | 70 | 1.15 | 0.129 |
| AND/NAND | -20 | 0.15 | 1.422 |
| | 70 | 1.15 | 0.135 |
| DFF | -20 | 0.442 | 2.97 |
| **Logic** | **Temperature** | **Power[nW]** | **Delay [µs]** |
| DFF | 70 | 3.366 | 0.152 |

**TABLE 1:** Power-Delay table for STSCL based logic gates

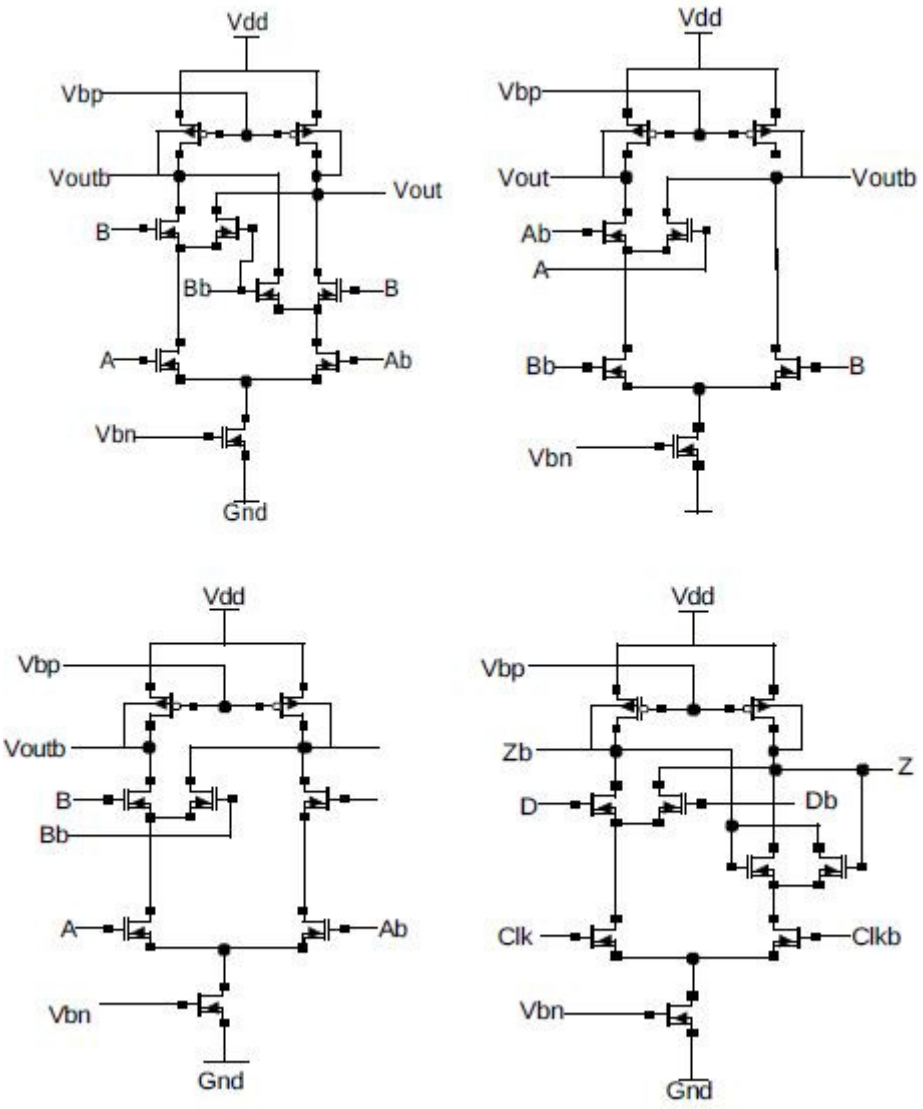


**FIGURE 1:** XOR/XNOR, OR/NOR, AND/NAND, DFF

### 2.1 Sub-threshold Amplifier for Bias Circuit [1]

Folded-cascode architecture has been used to design the amplifier required for the design of replica bias circuit. In Figure 2 shows a schematic view of the amplifier with modified PMOS load device [4]. Similar PMOS load devices have been used for the design of the amplifier's

architecture in order to operate it at sub-threshold region. Even-though this architecture uses more number of transistors but it can easily be applicable to operate at very low voltage. Other architectures like two-stage OTA can also be used which require less number of transistors but is difficult to be operated at sub-threshold regime.

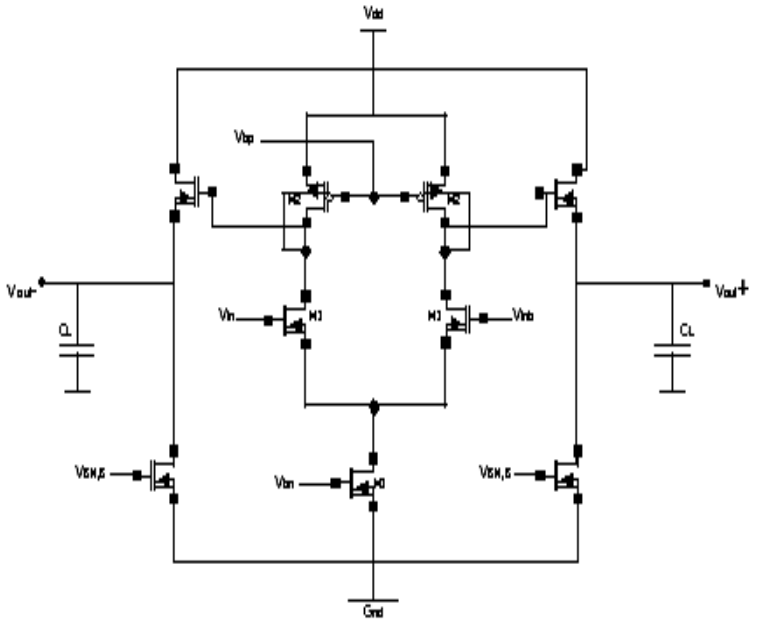


**FIGURE 2:** Folded-cascode amplifier (operates in sub-threshold region)

## 3. STSCL BASED FIR FILTER

The fifth order FIR filter designed in this paper is a conventional, widely-used and foremost verified structure (as in Figure 3). IIR filter can be also used instead of the FIR filter but IIR filters have more design complications compare to FIR filter. The filter has a of serial-input and serial-output form with a sampling frequency of 44.1 kHz, and for the multiplication with fixed coefficients a five-bit of serial/parallel multiplier [6] has been used. The response for the filter is given in Figure 4. The coefficients are represented in canonic signed digit (CSD) form. CSD is an optimized form compares to the more conventional two's complement form [5]. The CSD based S/P multiplier uses lesser hardware resources and hence lower the power down to further level.

The supply voltage is 0.2 V with a bias current at 250 pA per stage as discussed before. The supply voltage of 0.2 V is the limit up to which the system can be operated. The basic tryout for the different supplies allowed seeing how well a system could perform under critical situation while STSCL gates have been configured to run at their minimum operating specification. Simulations have been operated and compiled on Cadence Virtuoso v6.14, using both CMOS and STSCL at -20℃ and 70℃ temperature. The results of the PDP along with the delay for the fifth-order filter are shown in TABLE 2.

| Logic | STSCL | | CMOS | |
|---|---|---|---|---|
| Temp [℃] | -20 | 70℃ | -20℃ | 70℃ |
| PDP [fJ] | 600.4 | 45.81 | 784.6 | 46.23 |
| Delay [µs] | Value 8 | 1.06 | 5.65 | 0.67 |

**TABLE 2:** PDP values for STSCL and CMOS based Fifth-order FIR filter.

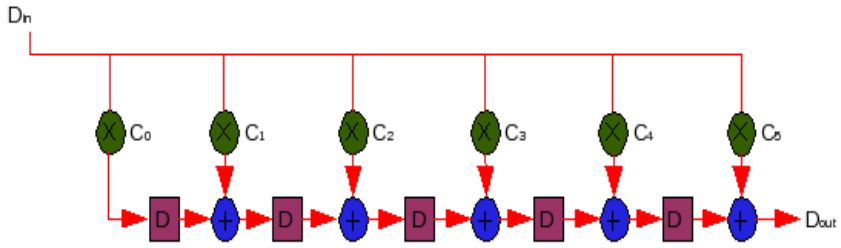


**FIGURE 3:** Fifth-order FIR Filter

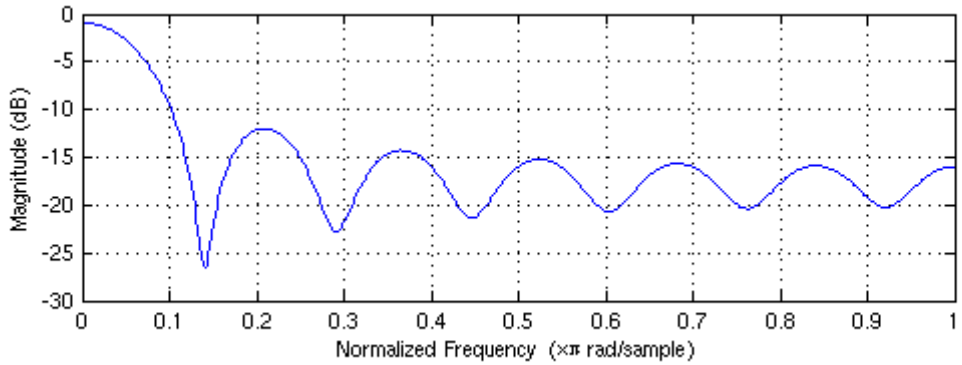


**FIGURE 4:** Response Fifth-order FIR Filter

## 4. CONCLUSION

The performance for STSCL at extreme condition is comparatively better than CMOS in a 45 nm process at a supply voltage of 0.2 V. The most important factor found in the simulations is that the energy consumption for STSCL is less than CMOS which suggests trying out further implementation of all the digital components of the sensor in STSCL.

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