Design and Implementation of Low Ripple Low Power Digital Phase-Locked Loop

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Abstract

We propose a phase-locked loop (PLL) architecture which reduces double frequency ripple without increasing the order of loop filter. Proposed architecture uses quadrature numerically–controlled oscillator (NCO) to provide two output signals with phase difference of $\pi/2$. One of them is subtracted from the input signal before multiplying with the other output of NCO. The system also provides stability in case the input signal has noise in amplitude or phase. The proposed structure is implemented using field programmable gate array (FPGA) which dissipates 15.44 mW and works at clock frequency of 155.8 MHz.

Keywords*:* Digital Phase-Locked Loop (DPLL), Field Programmable Gate Array (FPGA), Numerically-controlled Oscillator (NCO), Read Only Memory (ROM), Look-Up Table (LUT).

1. INTRODUCTION

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output phase and the phase of a reference input. It tracks the phase changes that are within its bandwidth. Tasks performed by PLL include carrier recovery, clock recovery, tracking filters, frequency and phase demodulation, phase modulation, frequency synthesis and clock synchronization. PLLs are also used in radio, television, every type of communications (wireless, telecom, datacom), all types of storage devices and noise cancellers [1].

A PLL block diagram is shown in Fig 1. It has three main components which are, phase detector (PD), a low pass filter (LPF) called as the loop filter and a voltage controlled oscillator (VCO). PLL operates as a negative feedback loop. VCO generates a signal at center frequency, multiplied by the input signal in PD and the resultant is passed through LPF to eliminate double frequency ripple. The filter output is fed back to VCO to adjust its generated frequency and phase. This process continues until no phase or frequency difference exists and the PLL is said to be “frequency locked”.

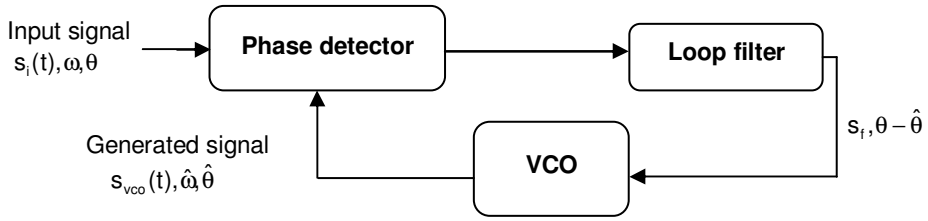

FIGURE 1: Phase Locked Loop

PLL behaves as a narrow band tracking filter and its LPF output has a characteristics of frequency discriminator. The linearity of VCO affects the overall linearity of PLL in case of analog implementation [2]. Hence, digital PLLs can solve some of the limitations of analog ones. In addition, the digital tangent method can compute frequency from the ratio of in-phase and quadrature (I-Q) signals [3,4,5]. Some other problems associated with the analog loops like sensitivity to d.c. drifts and the need for initial calibration and periodic adjustments can also be alleviated using DPLL. Nonuniform sampling DPLLs are the most ones because they are simple to implement and easy to model [6]. Digital tanlock loop (DTL), proposed in [7], has introduced several advantages over other nonuniform sampling digital phase locked loops. It allows a wider locking range of the first-order loop and a reduced sensitivity of the locking conditions to the variation of input signal power [7].

Noise is an extremely important issue in the field of PLL applications and is of two main types. Most common is the additive white Gaussian noise (AWGN) which is added to the signal at every component of communication system. Fig. 2 shows an input sinusoidal signal with AWGN at 35 dB signal to noise ratio (SNR). Second type of noise in PLL is called as the double frequency ripple, which is generated by phase detector. Since phase detector multiplies two sinusoidal signals, its output will be two terms, one is at low frequency and the other is at higher frequency (2ω). The situation will be critical when the two noise sources are involved with the feedback loop. This will affect the operation of PLL especially when it is used as a synthesizer, as the generated frequencies will have much noise or jitter.

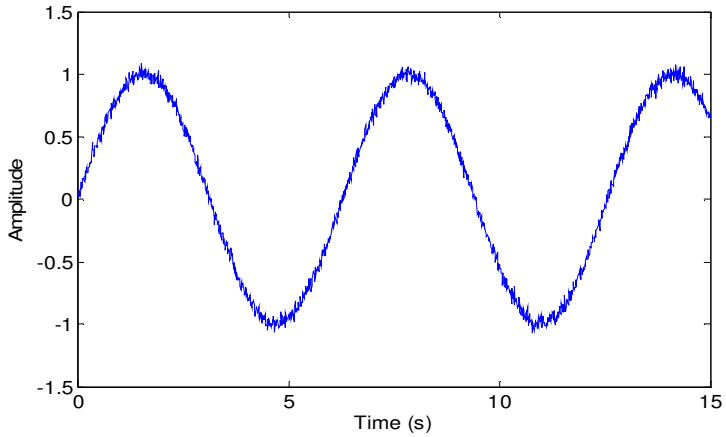

FIGURE 2: Input signal with AWGN at 35dB SNR

LPF in the loop is used to eliminate double frequency terms resulting from multiplying the input signal with generated signal from VCO. In practical circuits, there is no ideal LPF and a residual noise will be present at the output of phase detector. Using higher order loop filters offer better noise cancellation. However, in this case generally the PLL becomes unstable since its order is always higher by 1 than that of loop filter. Noise cancellation performance can also be improved

by lowering cut-off frequency of first order LPF. This will cause lower bandwidth and lower damping of the PLL and will also have a negative impact on its locking ability.
This paper presents an improved PLL which helps in suppressing noise without increasing the order of LPF. Computer simulations performed using Matlab show significant performance improvements over conventional PLL. Furthermore, the system is also modeled in VHDL and implemented using FPGA. This hardware implementation further confirms the results obtained through computer simulations.

2. Mathematical Analysis of PLL

In this section we'll perform mathematical analysis of a conventional PLL shown in Fig. 1. We assume an input sinusoidal signal

$$s_i(t) = A_i \sin(\omega t + \theta(t)) = A_i \sin\psi(t), \quad (1)$$

where ω is the angular frequency and $\theta(t)$ is the unknown phase of input signal. The signal generated by VCO is

$$s_{vco}(t) = A_o \cos(\hat{\omega} t + \hat{\theta}(t)) = A_i \cos\hat{\psi}(t), \quad (2)$$

where $\hat{\omega}$ is the estimation of angular frequency of VCO and $\hat{\theta}(t)$ is the estimated phase of VCO.

There are several designs and construction methods for phase detector. For the present discussion, we assume that PD is a multiplier. Input signal is multiplied by the VCO output, then

$$\begin{aligned} s_d(t) &= k_m s_i(t) \times s_{vco}(t) \\ &= \frac{A_i A_o k_m}{2}[\sin((\omega-\hat{\omega})t + \theta(t) - \hat{\theta}(t)) + \sin((\omega+\hat{\omega})t + \theta(t) + \hat{\theta}(t))] \\ &= k_d\,[\sin(\psi(t) - \hat{\psi}(t)) + \sin(\psi(t) + \hat{\psi}(t))], \end{aligned} \quad (3)$$

where k_m is the gain of phase detector with dimension [1/V], $k_d = \frac{A_i A_o k_m}{2}$.

In the simplest case we assume that low-pass filter removes the upper sideband with frequency $\omega+\hat{\omega}$ but passes the lower sideband $\omega-\hat{\omega}$. VCO's tuning voltage will be

$$s_f(t) = k_d \sin(\psi(t) - \hat{\psi}(t)) = k_d \sin\psi_e(t), \quad (4)$$

where $\psi_e(t)$ is the phase difference between input and output VCO signals

$$\psi_e(t) = \psi(t) - \hat{\psi}(t). \quad (5)$$

This difference will be used to control the frequency and phase generated by VCO. If the error signal is zero, VCO produces just its free running frequency (ω_c, center frequency). If the error signal is other than zero, then VCO responds by changing its operating frequency.

$$\hat{\omega}(t) = \omega_c + k_o s_f(t), \quad (6)$$

where the constant k_o is the gain of VCO in units (2πHz / V). After integration of the above equation and substituting into (5), the phase difference is

$$\psi_e(t) = \psi(t) - \omega_c - \int_{-\infty}^{t} k_o s_f(\tau)\, d\tau. \quad (7)$$

This can be rearranged as follows:

$$\psi_e(t) = \omega\, t - \omega_c t - \int_{-\infty}^{t} k_o k_d \sin\psi_e(\tau)\, d\tau. \tag{8}$$

Differentiating (8) w.r.t. 't' gives

$$\frac{d}{dt}\psi_e(t) = \Delta\omega - K\sin\psi_e(t) \tag{9}$$

where $\Delta\omega = \omega - \omega_c$ and $K = k_o k_d$ is the gain of PLL having units $[2\pi Hz]$.

The PLL continues to vary the phase of VCO $\hat{\omega}$ until locked, that is, frequency and phase of the input signal are the same as those generated by VCO. After getting locked, PLL follows the changes in frequency and phase of input signal [9,10].
It can be concluded from the above analysis that the phase lock arrangement is described by the nonlinear equation (9). Solution of this equation is not known for arbitrary values $\Delta\omega$, and k. Without an aperiodic solution, the feedback system (PLL) cannot achieve phase stability, i.e., output frequency of VCO $\hat{\omega}$ will never be equal to input frequency (ω). Simplifications are needed to solve the equation. One solution is the linear solution, in which we assume that, for small values of $\psi_e(t)$

$$\sin\psi_e(t) \approx \psi_e(t) \tag{10}$$

Substituting in (9)

$$\frac{d}{dt}\psi_e(t) = \Delta\omega - K\psi_e(t) \tag{11}$$

If $\frac{d}{dt}\theta(t) = 0$, solution of this differential equation is

$$\psi_e(t) = e^{-Kt}(\psi_{e0} - \frac{\Delta\omega}{K}) + \frac{\Delta\omega}{K} \tag{12}$$

where $\psi_{e0} = \psi_e(0) = \theta(0) - \hat{\theta}\,(0)$.
For steady state, that is, for $t \to \infty$, the left hand side of (11) is equal to zero, with the result that

$$\psi_{e\infty} = \frac{\Delta\omega}{K}. \tag{13}$$

In the above analysis we assumed that LPF completely suppressed the high frequency term in (3). This operation is not easy for a first order low pass filter and requires a higher order. However, the LPF is part of a feedback control system and instability of the system will increase in this case. Our proposed improvement of PLL aims to reduce noise inside the loop without using higher order LPF.

3. Proposed PLL

We propose modification in conventional PLL to suppress noise without increasing the order of LPF (first order LPF). Fig. 3 shows the block diagram of our suggested architecture. It uses a quadrature numerically controlled oscillator (NCO) to generate two signals $\sin(\hat{\omega}\,t+\hat{\theta}\,(t))$ and $\cos(\hat{\omega}\,t+\hat{\theta}\,(t))$. The phase detector subtracts $\sin(\hat{\omega}\,t+\hat{\theta}\,(t))$ from the input signal and multiplies the resultant by $\cos(\hat{\omega}\,t+\hat{\theta}(t))$ before passing on its output to LPF.

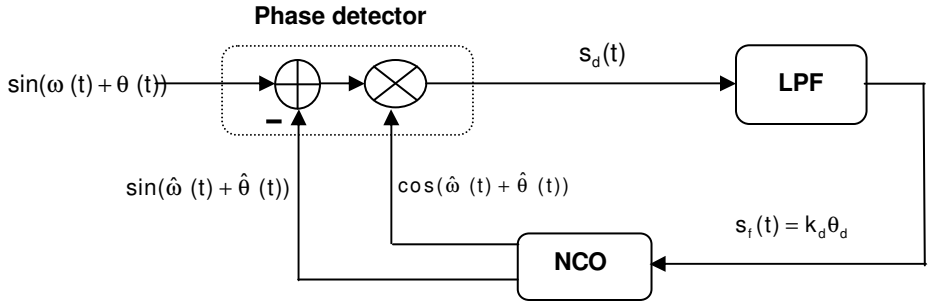

FIGURE 3: Block diagram of proposed PLL

This operation eliminates almost the entire high frequency term and if there is some residual, the first order LPF can remove it easily. Following equations describe the operation of proposed PLL in time domain.

Output signal from the phase detector is

$$\begin{aligned} s_d(t) &= k_d[\sin\psi\,(t)-\sin\hat{\psi}\,(t)]\cos\hat{\psi}\,(t) \\ &= k_d\,[\sin(\psi\,(t)-\hat{\psi}\,(t))+\sin(\psi\,(t)+\hat{\psi}\,(t))-\sin(2\,\hat{\psi}\,(t)] \end{aligned} \tag{14}$$

A comparison of (3) and (14) clearly establishes that in the proposed structure, the high frequency term $\sin(\psi\,(t)+\hat{\psi}\,(t))$ is subtracted by the term $\sin(2\,\hat{\psi}\,(t))$ before passing on the resultant to LPF. Thus even a first order LPF can suppress the noise easily. In conventional PLL, LPF is responsible for removing the term $\sin(\psi\,(t)+\hat{\psi}\,(t))$. First order filter cannot suppress all this term and its output will have large residual high frequency component.

Proposed modification will not have any negative impact on the PLL's locking performance. The term $k_d \sin\psi_e(t)$ is passed to VCO and the process continues like a conventional PLL.

4. Simulation Results

In this section we compare the performances of proposed and conventional PLL's using computer simulations. Two types of simulations are done. In the first group of simulations, we use a first order LPF in both architectures. Both architectures receive a signal with frequency difference (results shown in Fig. 4), phase difference, or both frequency and phase are changed (results shown in Fig. 6). In the second group of simulations, proposed PLL uses a first order LPF, while conventional PLL uses a second order LPF and performances of the two are compared.

4.1 Proposed versus Conventional PLL (Using first order LPF)

The parameters for both PLLs are:

$k_m = 1\ v^{-1}$, $k_o = 1500$ rad / v.s, $f_s = 1.0\times10^5$ Hz, $f_{vco}=1.0\times10^4$ Hz.

LPF: first order with cut-off frequency =1000 Hz,

VCO generates $s_{vco}(t) = \cos(2\pi f_{vco} t)$

First of all we perform comparison of the two PLL structures in case of input signal having frequency difference. For $\omega = 2\pi\times10100$ rad/s and $\theta(t) = 0$ in (1), Fig. 4 shows the response of both PLLs for the input signal. It can be seen that the proposed PLL suppresses much more noise than the conventional one. In Fig. 4 the response of proposed PLL converges to the mean value 0.0389 with variance 1.3926×10^{-4}. While the conventional PLL has the mean value 0.0389 with a high variance of 4.4758×10^{-4}.

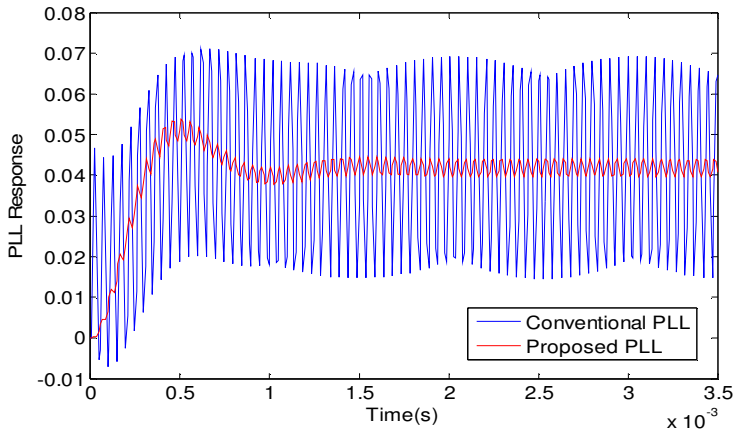

FIGURE 4: Response in case of frequency difference

Fig. 5 shows amplitude spectrum of output signals from each phase detector and each LPF for the two architectures. As can be seen in Fig. 5(a) the proposed architecture attenuates the high frequency term at $f = 2\times10^4$ Hz to an amplitude of 0.05 V before passing signal to the LPF which eliminates this term completely as shown in Fig. 5(b). While in conventional PLL the amplitude of high frequency term is 10 V which is almost equal to the amplitude of low frequency term. After passing signal through LPF high frequency component residual noise still has amplitude of 0.025 V as shown in Fig. 5(d).

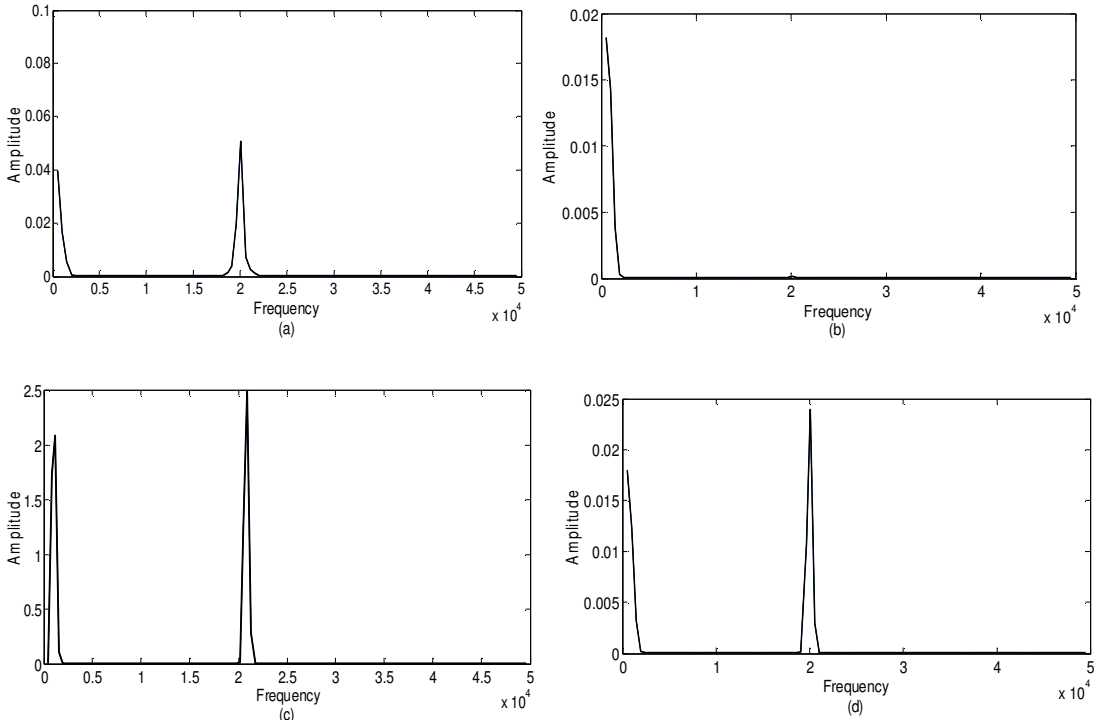

FIGURE 5: Amplitude spectrum of the output signal of (a) PD in proposed PLL, (b) LPF in proposed PLL, (c) PD in conventional PLL, (d) LPF in conventional PLL.

We also performed comparison in case of input signal having both frequency and phase difference. Fig. 6 illustrates the response of both architectures at $\omega = 2\pi \times 10100$ rad/s and $\theta(t) = \pi / 2$ in (1).

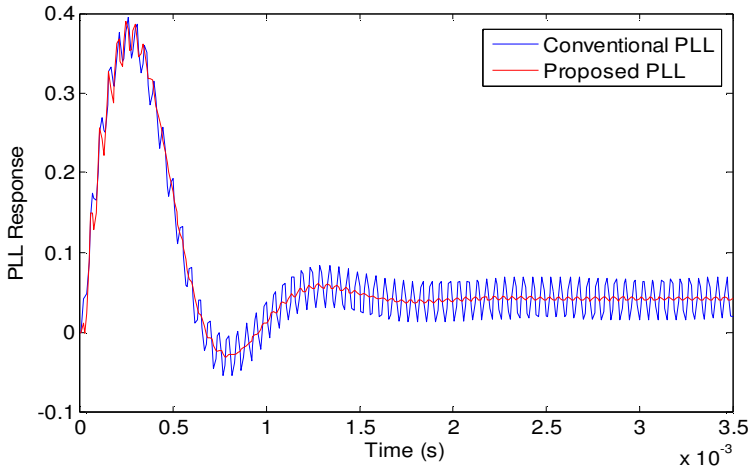

FIGURE 6: Response in case of phase difference

We also performed comparison of the two structures in the presence of AWGN. When the input signal is combined with AWGN at 35 dB SNR, the response of both PLLs is plotted in Fig. 7.

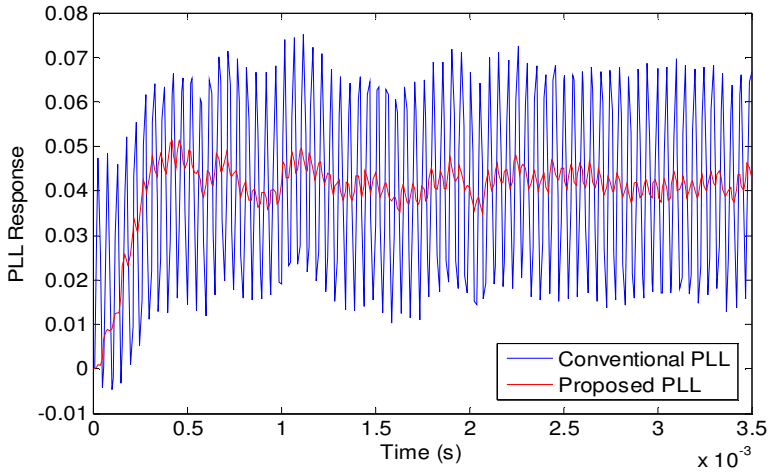

FIGURE 7: Response in the presence of AWGN at 35 dB SNR

4.2 Proposed PLL versus Higher Order Conventional PLL

In this group of simulations, we have used a first order LPF in the proposed PLL while second order LPF is used in conventional one. Fig. 8 shows both responses when the frequency of input signal is changed and the phase stays fixed, i.e, $\omega = 2\pi \times 10100$ rad/s and $\theta(t) = 0$.

Proposed PLL locked to the input signal while conventional PLL did not achieve locking although noise level is reduced. As mentioned before, increasing the order of LPF in the loop increases instability of the system. Therefore, the parameters of conventional PLL must be adjusted carefully to control the location of poles and zeros to achieve stability of higher order PLLs.

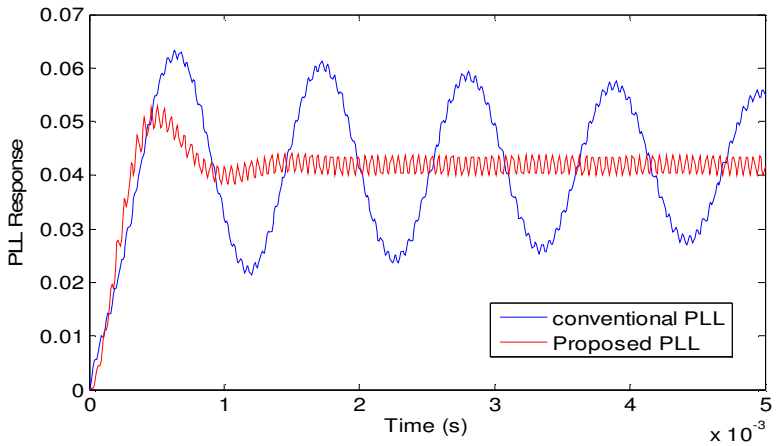

FIGURE 8: Response when conventional PLL has higher order LPF than proposed one

The above simulations clarify and explain operation of the proposed architecture through a comparison with conventional one in different cases such as a frequency difference or phase difference in the input signal as shown in both Fig. 4 and Fig. 6. Furthermore simulations show us the signals' amplitudes in different stages inside both architectures as in Fig. 5. The situation in case the received signal has AWGN is clarified in Fig. 7. In case the order of LPF in conventional PLL is increased, Fig. 8 shows that the noise is suppressed while the PLL loses stability and

unlocked the input signal while proposed one is stable. All previous simulations clearly demonstrate that the proposed PLL has low ripple and is more stable than the conventional one.

5. Hardware Implementation of Proposed PLL

Since Digital Phase Locked Loops (DPLL) find applications in most of the state of the art equipment, we discuss hardware implementation of the digital version of our proposed architecture in this section. Hardware modeling is performed using VHDL language [11,12]. In Fig. 3, the input signal is 8 bits-length, comes from Analog to digital converter (ADC) and generates 8 bits as an output of DPLL architecture. The following sub blocks describe the operation of each part:

5.1 Phase detector (PD)

The Phase Detector detects the phase error between input signal and generated signal from NCO. This operation is done using a multiplier and a register as shown in Fig. 9. In the VHDL model, Booth's multiplication algorithm [13] is used to achieve smaller area and higher speed of multiplication.

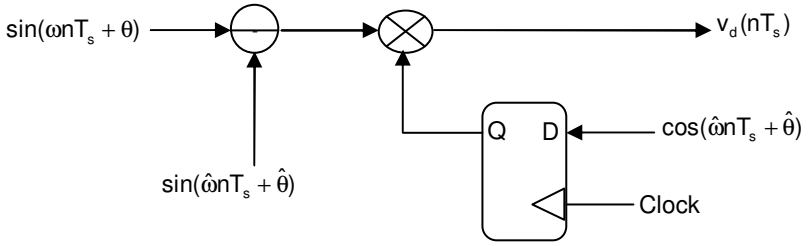

FIGURE 9: Phase Detector module

5.2 Loop Filter

The loop filter is a digital filter responsible for eliminating high frequency term from the output of phase detector unit. The filter is a first order IIR low pass filter. In designing filter it is important to choose the pole, which controls cut-off frequency, to be inside the unit circle to provide stability to the filter. It cannot be equal to 1 because the filter in this case becomes an integrator [14,15]. The transfer function of the filter in z-domain for an input $s_d(nT_s)$ and output $s_f(nT_s)$ is

$$H(z) = \frac{s_f(z)}{s_d(z)} = \frac{kz^{-1}}{1 - pz^{-1}} \tag{15}$$

where k, and p are coefficients of the filter. The structure of digital filter is illustrated in Fig. 10.

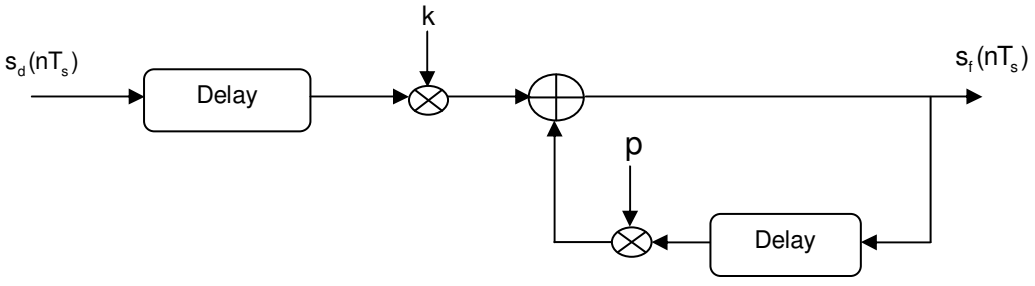

FIGURE 10: First order digital low pass filter

5.3 Quadrature NCO

NCO is an important component in DPLL because it determines power consumption of the entire system. The generation of analog sinusoidal waveform in digital domain requires storing the amplitudes of analog waveform in a read only memory (ROM). The structure of ROM in digital implementation causes high power consumption and slow operation of the circuit. These drawbacks of ROM block limit the use of DPLL in portable applications which require low power consumption [16].

Since it is desirable to have a large number of bits to achieve fine frequency tuning, several techniques have been invented to limit the ROM size while maintaining sufficient performance. One method exploits the quarter wave symmetry of the sine function to reduce by four the number of angles for which a sine amplitude is required. Truncating the phase accumulator output (eliminating a number of most significant bits (MSB) of the output) is another common method, although it introduces spurious harmonics in the generated waveform [17].

Various angular methods have been proposed to reduce memory size [18-19]. They consist of splitting the ROM into a number of smaller units each addressed by a portion of the truncated phase accumulator output bits. Data retrieved from each small ROM is added to yield a sinusoidal approximation.

In this paper instead of using ROM in the quadrature NCO, piecewise linear approximation for the first quarter of the sine waveform is employed. From the first quarter of sine wave a complete waveform for sine and cosine can be generated due to symmetry of both functions. The first quarter of sine waveform which lies between $(0,\pi/2)$ is represented by eight linear equations. Slopes and constants for these linear equations are chosen according to minimum mean square error (MMSE) criterion between the approximated and ideal sine wave.

$$\sin(t) \approx a_i t + b_i, \qquad \frac{i}{16}\pi \le t < \frac{i+1}{16}\pi, \qquad i = 0,1....7 \tag{16}$$

where a_i is segment slope and b_i is segment constant.

The quadrature NCO block diagram is shown in Fig.11. It consists of 3 blocks, the first one is the accumulator, which receives input signal $s_f(nT_s)$ corresponding to phase difference between θ and $\hat{\theta}$. The accumulator width is 16 bits.

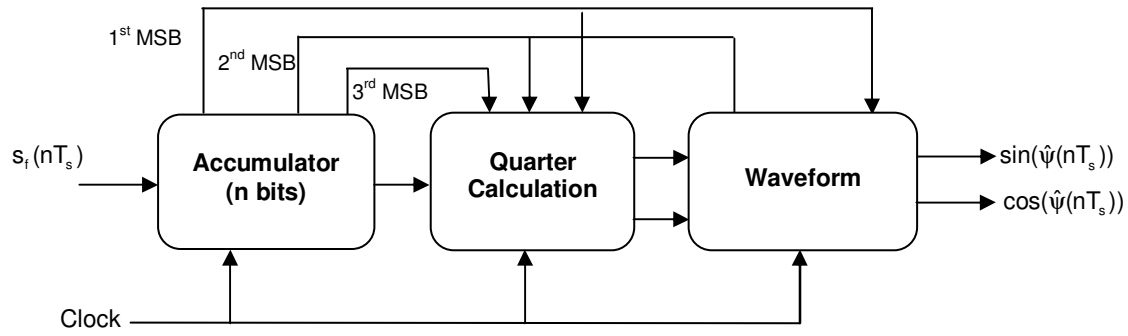

FIGURE 11: Structure of modified NCO

The accumulator works as a circular counter, a complete rotation of accumulator represents one cycle of output waveform. All bits leaving accumulator are directed to Quarter calculation block. The first three MSBs are used to choose between slopes and constants for every linear segment. After calculation of first quarter, the results are directed to waveform block. This block forms

complete sine and cosine waveforms according to the 1st MSB and 2nd MSB of accumulator block. The frequency of generated waveforms f_{nco} is

$$f_{nco} = (\frac{s_f + \omega_c}{2^n}) \times f_{clk}, \quad (17)$$

where f_{nco} is the generated frequency, s_f are the input binary bits to the NCO, ω_c is a constant value which represents the free running frequency of NCO, n is number of bits or width of accumulator which is 16 bits and f_{clk} is the clock frequency which is 50 MHz. When input signal s_f is zero, the architecture generates free running frequency.

Spurious free dynamic range (SFDR) is a measure of spectral purity of the waveform generated by NCO. It represents the ratio between amplitude of the fundamental generated frequency and the amplitude of the largest spur in the dynamic range of NCO $(0 : f_s/2)$ [20,21]. For our proposed NCO, SFDR is 60 dBc which is sufficient not to introduce ripples to DPLL.

Fig. 12 shows the output spectrum for input word of value 1317 representing $v_f(n)$, at a clock frequency of 50 MHz, ω_c=1317 and accumulator width n = 16. The fundamental frequency is approximately 2 MHz with -30.057 dB and the spurious appears at 14.46 MHz with -89.925 dB, so SFDR = 59.868 dBc.

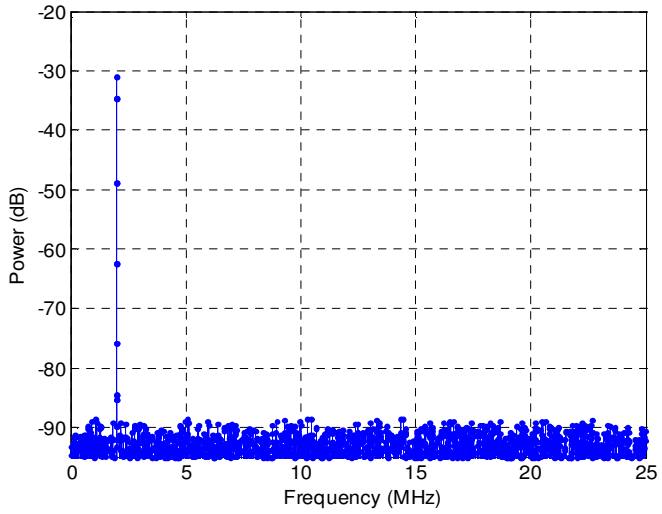

FIGURE 12: SFDR in dBc of fundamental frequency 2 MHz

6. FPGA Implementation Results

The proposed DPLL architecture is written in VHDL and simulated using Modelsim program. The simulation is done at clock frequency 50 MHz, the input is sinusoidal waveform of frequency 1 MHz. Fig. 13 shows the simulation waveforms for proposed PLL. The input signal is multiplied by the modified NCO signal after subtracting the other sinusoidal output from NCO and the resultant is subjected to digital filter. The final output shows that digital simulation agrees with the expected waveform. Fig. 14 shows the response of conventional PLL for the same input signal. It is clear that the proposed PLL suppresses noise more effectively than the conventional one.

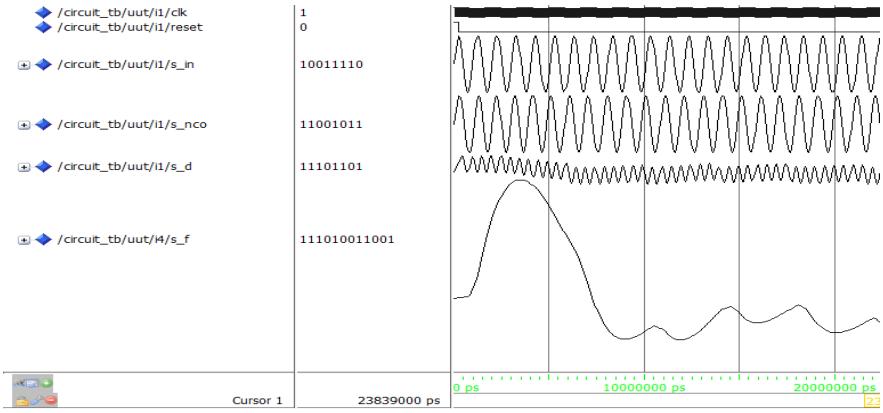

FIGURE 13: Proposed DPLL waveforms for input sinusoidal of 1 MHz

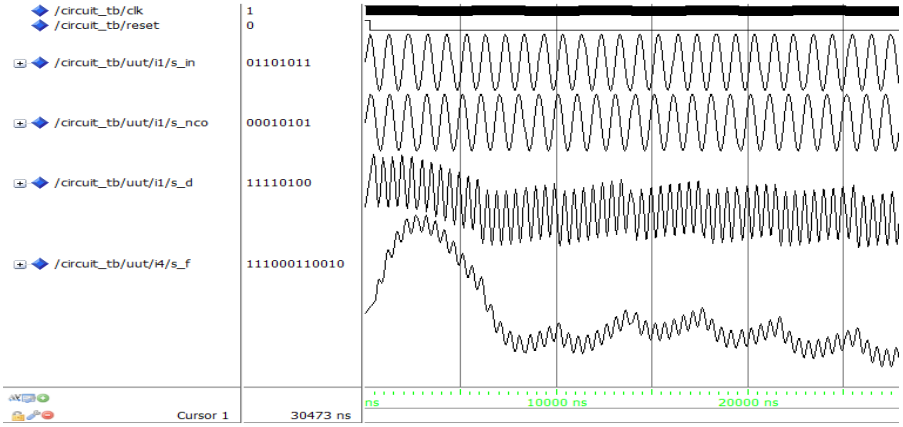

FIGURE 14: Conventional DPLL waveforms for input sinusoidal of 1 MHz

A comparison between conventional DPLL (in which the phase detector is only a multiplier and NCO uses ROM) and proposed DPLL is done by implementing both architectures on the same FPGA device (cyclone II, EP2C35F67C). The result is illustrated in TABLE 1. It is clear that the proposed PLL saves area, reduces power consumption and works at higher frequency than the conventional one.

Architecture	Conventional DPLL	Proposed DPLL
Total logic elements	762	655
Logic registers	106	78
Memory bits	2048	0
Maximum clock	115.02 MHz	155.8 MHz
Core dynamic power consumption(100 MHz)	19.54 mW	15.44 mW

TABLE 1: DPLL implementation comparison

7. CONSLUSION

An improved PLL design was presented. The signal estimated by the VCO was subtracted from the signal input to the PLL, before passing the resultant to the phase detector. This resulted in

eliminating the noise present because of the double frequency ripple, without increasing order of the LPF. Computer simulations performed using Matlab showed significant performance improvements in the case of changing frequency, phase and both frequency and phase. A digital version of the improved PLL was also proposed using VHDL and then implemented through FPGA. High power consumption and low operation speed in conventional DPLL results because of the NCO in which the generation of sinusoidal waveform depends on ROM. As accuracy of the generated signal increases, the size of ROM is increased. Proposed structure replaces the traditional NCO with another one, which depends on piecewise linear approximation to the sine function thus ROM is not needed in this case. The proposed architecture reduces noise, power consumption, area consumption and works at higher frequency than the conventional DPLL.

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